

# MCUXpresso SDK Documentation Release 25.09.00-pvw1



NXP Jul 17, 2025

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		Power Driver
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		SPI Driver
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This documentation contains information specific to the lpcxpresso 802 board.

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### **Chapter 1**

## LPCXpresso802

#### 1.1 Overview

LPC800 series boards and devices are fully supported by NXPs MCUXpresso suite of free software and tools, which include an Eclipse-based IDE, configuration tools and extensive SDK drivers/examples available at https://mcuxpresso.nxp.com. All boards in this series include an on-board CMSIS-DAP debug probe based on the LPC11U35 debug probe, with the option for an external debug probe such as those from SEGGER and PE Micro. Popular Arduino UNO shield boards can be used on these boards, enabling quick and easy prototyping. The LPC800 series is fully supported by NXPs 'MCUXpresso suite <a href="https://www.nxp.com/mcuxpresso>"https://www.nxp.com/mcuxpresso>"https://www.nxp.com/mcuxpresso>"https://www.nxp.com/mcuxpresso>"https://www.nxp.com/mcuxpresso>"https://www.nxp.com/mcuxpresso>"https://wcuxpresso.nxp.com. MCUXpresso SDK includes project files for use with IDEs from lead partners Keil and IAR, and these IDEs are also fully supported by the MCUXpresso pin, clock and peripheral configuration tools.



MCU device and part on board is shown below:

• Device: LPC802

• PartNumber: LPC802M001JDH20

#### 1.2 Getting Started with MCUXpresso SDK Package

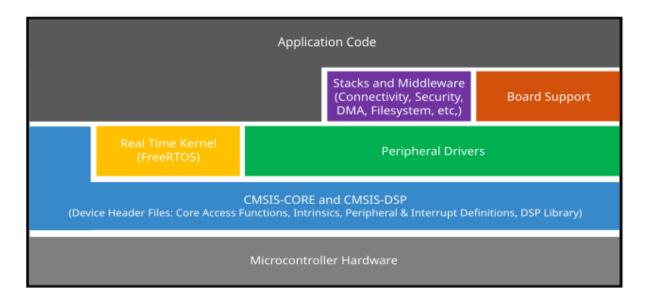
#### 1.2.1 Getting Started with MCUXpresso SDK Package

#### **Overview**

The NXP MCUXpresso software and tools offer comprehensive development solutions designed to optimize, ease, and help accelerate embedded system development of applications based on general purpose, crossover, and Bluetooth-enabled MCUs from NXP. The MCUXpresso SDK includes a flexible set of peripheral drivers designed to speed up and simplify development of

embedded applications. Along with the peripheral drivers, the MCUXpresso SDK provides an extensive and rich set of example applications covering everything from basic peripheral use case examples to full demo applications. The MCUXpresso SDK contains optional RTOS integrations such as FreeRTOS and Azure RTOS, and various other middleware to support rapid development.

For supported toolchain versions, see *MCUXpresso SDK Release Notes* (document MCUXSDKRN). For more details about MCUXpresso SDK, see MCUXpresso Software Development Kit (SDK).



#### MCUXpresso SDK board support package folders

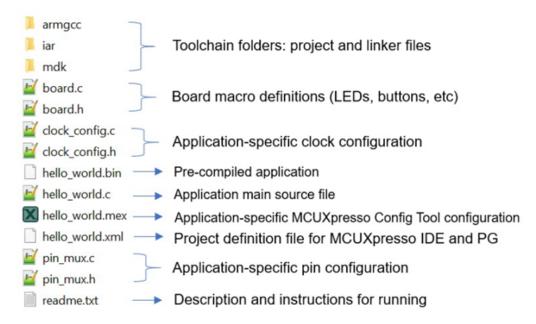
MCUXpresso SDK board support package provides example applications for NXP development and evaluation boards for Arm Cortex-M cores including Freedom, Tower System, and LPCX-presso boards. Board support packages are found inside the top-level boards folder and each supported board has its own folder (an MCUXpresso SDK package can support multiple boards). Within each <br/>
<br/>board\_name> folder, there are various subfolders to classify the type of examples it contains. These include (but are not limited to):

- cmsis\_driver\_examples: Simple applications intended to show how to use CMSIS drivers.
- demo\_apps: Full-featured applications that highlight key functionality and use cases of the target MCU. These applications typically use multiple MCU peripherals and may leverage stacks and middleware.
- driver\_examples: Simple applications that show how to use the MCUXpresso SDK's peripheral drivers for a single use case. These applications typically only use a single peripheral but there are cases where multiple peripherals are used (for example, SPI conversion using DMA).
- emwin examples: Applications that use the emWin GUI widgets.
- rtos\_examples: Basic FreeRTOS OS examples that show the use of various RTOS objects (semaphores, queues, and so on) and interfaces with the MCUXpresso SDK's RTOS drivers
- usb\_examples: Applications that use the USB host/device/OTG stack.

**Example application structure** This section describes how the various types of example applications interact with the other components in the MCUXpresso SDK. To get a comprehensive understanding of all MCUXpresso SDK components and folder structure, see *MCUXpresso SDK API Reference Manual*.

Each <code><board\_name></code> folder in the boards directory contains a comprehensive set of examples that are relevant to that specific piece of hardware. Although we use the <code>hello\_world</code> example (part of the <code>demo\_apps</code> folder), the same general rules apply to any type of example in the <code><board\_name></code> folder.

In the hello\_world application folder you see the following contents:



All files in the application folder are specific to that example, so it is easy to copy and paste an existing example to start developing a custom application based on a project provided in the MCUXpresso SDK.

**Locating example application source files** When opening an example application in any of the supported IDEs, various source files are referenced. The MCUXpresso SDK devices folder is the central component to all example applications. It means that the examples reference the same source files and, if one of these files is modified, it could potentially impact the behavior of other examples.

The main areas of the MCUXpresso SDK tree used in all example applications are:

- devices/<device\_name>: The device's CMSIS header file, MCUXpresso SDK feature file, and a few other files
- devices/<device name>/cmsis drivers: All the CMSIS drivers for your specific MCU
- devices/<device\_name>/drivers: All of the peripheral drivers for your specific MCU
- $devices/< device\_name>/< tool\_name>$ : Toolchain-specific startup code, including vector table definitions
- devices/<device\_name>/utilities: Items such as the debug console that are used by many of the example applications
- devices/<devices\_name>/project: Project template used in CMSIS PACK new project creation

For examples containing middleware/stacks or an RTOS, there are references to the appropriate source code. Middleware source files are located in the middleware folder and RTOSes are in the rtos folder. The core files of each of these are shared, so modifying one could have potential impacts on other projects that depend on that file.

#### Run a demo using MCUXpresso IDE

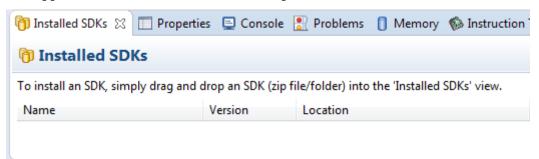
**Note:** Ensure that the MCUXpresso IDE toolchain is included when generating the MCUXpresso SDK package.

This section describes the steps required to configure MCUXpresso IDE to build, run, and debug example applications. The hello\_world demo application targeted for the hardware platform is used as an example, though these steps can be applied to any example application in the MCUX-presso SDK.

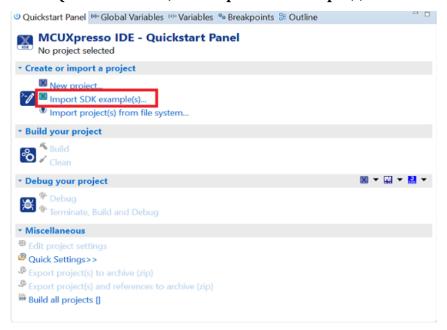
**Select the workspace location** Every time MCUXpresso IDE launches, it prompts the user to select a workspace location. MCUXpresso IDE is built on top of Eclipse which uses workspace to store information about its current configuration, and in some use cases, source files for the projects are in the workspace. The location of the workspace can be anywhere, but it is recommended that the workspace be located outside the MCUXpresso SDK tree.

**Build an example application** To build an example application, follow these steps.

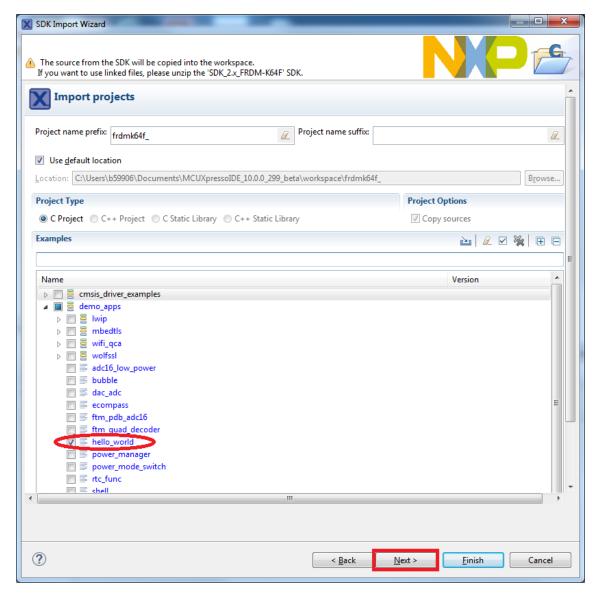
1. Drag and drop the SDK zip file into the **Installed SDKs** view to install an SDK. In the window that appears, click **OK** and wait until the import has finished.



2. On the Quickstart Panel, click Import SDK example(s)....



- 3. Expand the  $demo\_apps$  folder and  $select \ hello\_world$ .
- 4. Click Next.



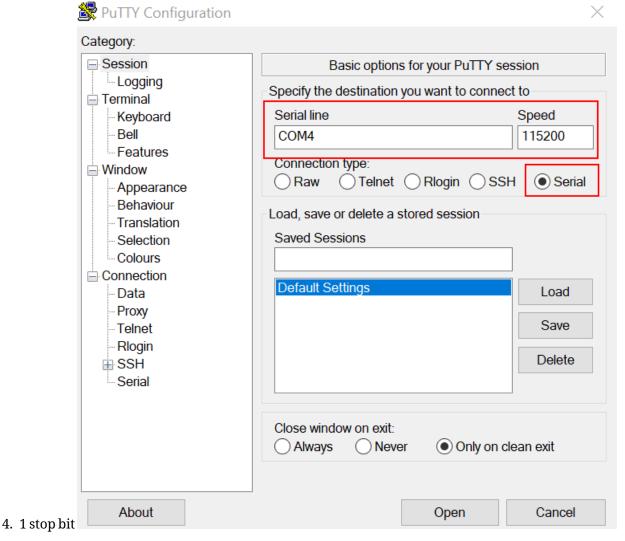
5. Ensure **Redlib:** Use floating-point version of printf is selected if the example prints floating-point numbers on the terminalfor demo applications such as adc\_basic, adc\_burst, adc\_dma, and adc\_interrupt. Otherwise, it is not necessary to select this option. Then, click **Finish**.

**Run an example application** For more information on debug probe support in the MCUX-presso IDE, see community.nxp.com.

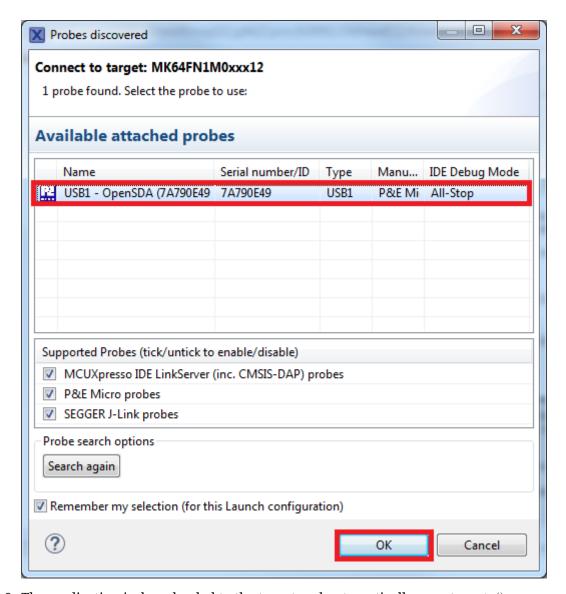
To download and run the application, perform the following steps:

- 1. Ensure the host driver for the debugger firmware has been installed. See *On-board debugger*.
- 2. Connect the development platform to your PC via a USB cable.
- 3. Open the terminal application on the PC, such as PuTTY or TeraTerm, and connect to the debug serial port number (to determine the COM port number, see *How to determine COM port*. Configure the terminal with these settings:
  - 1. 115200 or 9600 baud rate, depending on your board (reference BOARD\_DEBUG\_UART\_BAUDRATE variable in board.h file)
  - 2. No parity

3. 8 data bits



- 4. On the **Quickstart Panel**, click **Debug** to launch the debug session.
- 5. The first time you debug a project, the **Debug Emulator Selection** dialog is displayed, showing all supported probes that are attached to your computer. Select the probe through which you want to debug and click **OK**. (For any future debug sessions, the stored probe selection is automatically used, unless the probe cannot be found.)



- 6. The application is downloaded to the target and automatically runs to main().
- 7. Start the application by clicking **Resume**.

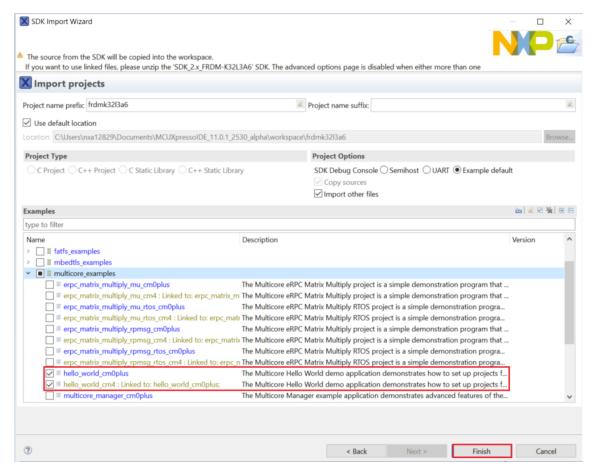


The  ${\it hello\_world}$  application is now running and a banner is displayed on the terminal. If not, check your terminal settings and connections.

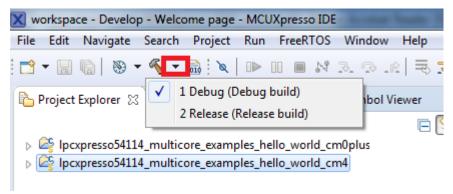


**Build a multicore example application** This section describes the steps required to configure MCUXpresso IDE to build, run, and debug multicore example applications. The following steps can be applied to any multicore example application in the MCUXpresso SDK. Here, the dual-core version of hello\_world example application targeted for the LPCXpresso54114 hardware platform is used as an example.

- 1. Multicore examples are imported into the workspace in a similar way as single core applications, explained in **Build an example application**. When the SDK zip package for LPCXpresso54114 is installed and available in the **Installed SDKs** view, click **Import SDK example(s)...** on the Quickstart Panel. In the window that appears, expand the **LPCxx** folder and select **LPC54114J256**. Then, select **lpcxpresso54114** and click **Next**.
- 2. Expand the multicore\_examples/hello\_world folder and select **cm4**. The cm0plus counterpart project is automatically imported with the cm4 project, because the multicore examples are linked together and there is no need to select it explicitly. Click **Finish**.

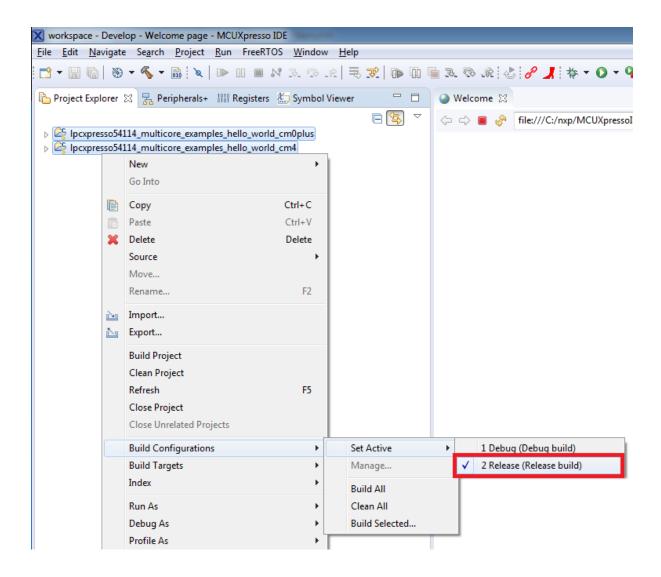


3. Now, two projects should be imported into the workspace. To start building the multicore application, highlight the <code>lpcxpresso54114\_multicore\_examples\_hello\_world\_cm4</code> project (multicore master project) in the Project Explorer. Then choose the appropriate build target, **Debug** or **Release**, by clicking the downward facing arrow next to the hammer icon, as shown in the figure. For this example, select **Debug**.

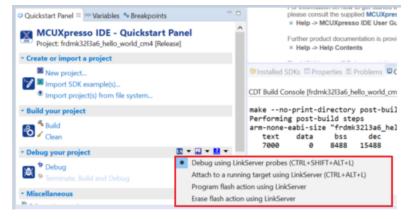


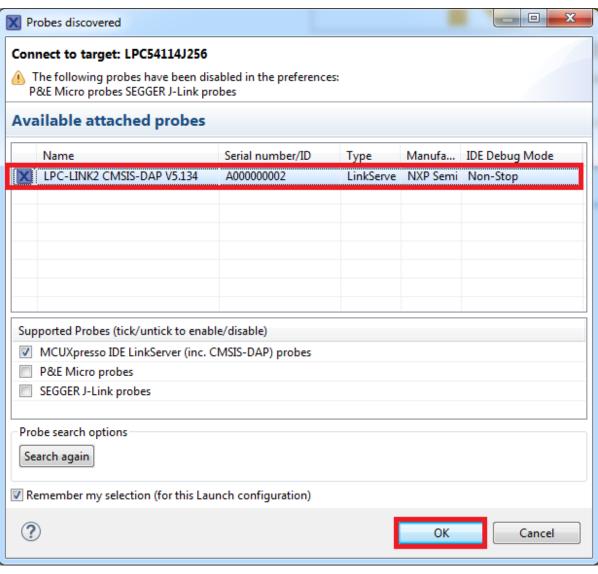
The project starts building after the build target is selected. Because of the project reference settings in multicore projects, triggering the build of the primary core application (cm4) also causes the referenced auxiliary core application (cm0plus) to build.

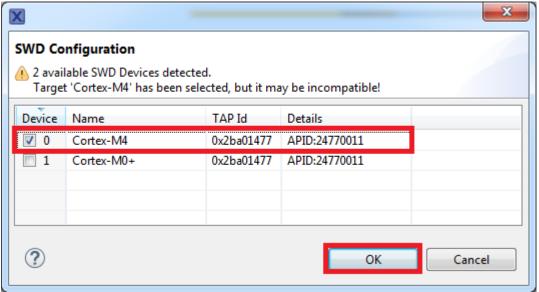
**Note:** When the **Release** build is requested, it is necessary to change the build configuration of both the primary and auxiliary core application projects first. To do this, select both projects in the Project Explorer view and then right click which displays the context-sensitive menu. Select **Build Configurations** -> **Set Active** -> **Release**. This alternate navigation using the menu item is **Project** -> **Build Configuration** -> **Set Active** -> **Release**. After switching to the **Release** build configuration, the build of the multicore example can be started by triggering the primary core application (cm4) build.



Run a multicore example application The primary core debugger handles flashing of both the primary and the auxiliary core applications into the SoC flash memory. To download and run the multicore application, switch to the primary core application project and perform all steps as described in Run an example application. These steps are common for both single-core applications and the primary side of dual-core applications, ensuring both sides of the multicore application are properly loaded and started. However, there is one additional dialogue that is specific to multicore examples which requires selecting the target core. See the following figures as reference.







```
🗶 workspace - Develop - lpcxpresso54114_multicore_examples_hello_world_cm4/source/hello_world_core0.c - MCUXpresso IDE
File Edit Source Refactor Navigate Search Project Run FreeRTOS Window Help
🏇 Debug 🏻
      ■ Ipcxpresso54114_multicore_examples_hello_world_cm4 Debug [C/C++ (NXP Semiconductors) MCU Application]
8

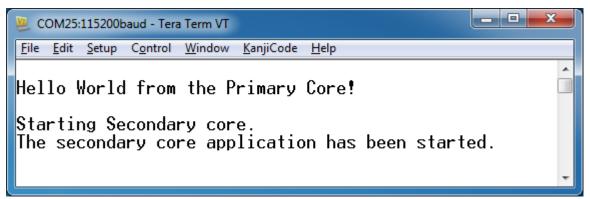
■ ipcxpresso54114_multicore_examples_hello_world_cm4.axf [LPC54114J256 (cortex-m0plus)]

 묾

■ Thread #11 (Stopped) (Suspended: Breakpoint)

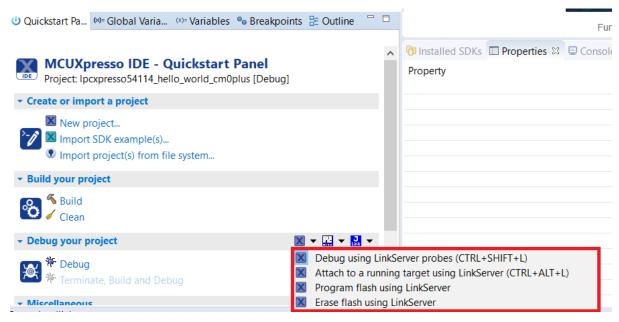
1010
0101
                main() at hello_world_core0.c:85 0x98a
*
           arm-none-eabi-gdb (7.12.0.20161204)
 8
     ic hello_world_core0.c ⋈
 (1)
       68 {
(x)=
       69
               uint32_t core1_image_size;
(x)=
       70 #if defined(__CC_ARM)
 0
               core1_image_size = (uint32_t)&Image$$CORE1_REGION$$Length;
       71
       72 #elif defined(__ICCARM__)
믊
                               _sec_core"
       73
           #pragma section = "
               core1_image_size = (uint32_t)__section_end("__sec_core") - (uint32_t)&core1_image_start;
        74
        75
           #endif
        76
               return core1_image_size;
        77 }
        78 #endif
       80 * @brief Main function
81 */
       820 int main(void)
       83 {
                /* Define the init structure for the switches*/
       gpio_pin_config_t sw_config = {kGPIO_DigitalInput, 0};
        86
        87
                /* Init board hardware.*/
        88
                /* attach 12 MHz clock to FLEXCOMM0 (debug console) */
               CLOCK AttachClk(kFR012M to FLEXCOMM0);
        89
        90
        91
               BOARD InitPins Core0();
               BOARD BootClockFROHF48M();
        92
        93
               BOARD_InitDebugConsole();
        94
        95
               /* Init switches */
               GPIO_PinInit(BOARD_SW1_GPIO, BOARD_SW1_GPIO_PORT, BOARD_SW1_GPIO_PIN, &sw_config);
        96
        97
               GPIO_PinInit(BOARD_SW2_GPIO, BOARD_SW2_GPIO_PORT, BOARD_SW2_GPIO_PIN, &sw_config);
```

After clicking the "Resume All Debug sessions" button, the hello\_world multicore application runs and a banner is displayed on the terminal. If this is not the case, check your terminal settings and connections.



An LED controlled by the auxiliary core starts flashing, indicating that the auxiliary core has been released from the reset and running correctly. It is also possible to debug both sides of the multicore application in parallel. After creating the debug session for the primary core, perform same steps also for the auxiliary core application. Highlight the lpcxpresso54114\_multicore\_examples\_hello\_world\_cm0plus project (multicore slave project) in the Project Explorer. On the Quickstart Panel, click "Debug 1pcxpresso54114\_multicore\_examples\_hello\_world\_cm0plus' [Debug]" to launch the second debug

#### session.



```
📈 workspace - Develop - Ipcxpresso54114_multicore_examples_hello_world_cm4/source/hello_world_core0.c - MCUXpresso IDE
<u>File Edit Source Refactor Navigate Search Project Run FreeRTOS Window Help</u>
  O ▼ ※ 👢 🗞 : 🐍 : ∅. ∅ ▼ 📠 : □ • (i) | (i) ▼ : □ • (i) • (ii) 
            🏇 Debug 🏻

■ Ipcxpresso54114_multicore_examples_hello_world_cm4 Debug [C/C++ (NXP Semiconductors) MCU Application]

 6

■ ipcxpresso54114_multicore_examples_hello_world_cm4.axf [LPC54114J256 (cortex-m0plus)]

  묾
                           Thread #1 1 (Stopped) (Suspended : Breakpoint)
  1010
0101
                                    main() at hello world core0.c:85 0x98a
  *
                         arm-none-eabi-gdb (7.12.0.20161204)

■ Ipcxpresso54114_multicore_examples_hello_world_cm0plus Debug [C/C++ (NXP Semiconductors) MCU Application]

■ Propresso54114_multicore_examples_hello_world_cm0plus.axf [LPC54114J256 (cortex-m0plus)]

  8
                          Thread #1 1 (Stopped) (Suspended: Signal: SIGSTOP:Stopped (signal))
  ψ
                                    0x1ec
 (x)=
                                    <signal handler called>() at 0xfffffff9
 (x)=
                                    0x0
  0
                        arm-none-eabi-gdb (7.12.0.20161204)
  먎
             🖟 hello_world_core0.c 🏻
                 68
                                  uint32_t core1_image_size;
                         #if defined(__CC_ARM)
                 70
                                  core1_image_size = (uint32_t)&Image$$CORE1_REGION$$Length;
                 71
                         #elif defined(_ICCARM_)
#pragma section = "__sec_core"
                 72
                 73
                 74
                                  core1_image_size = (uint32_t)__section_end("__sec_core") - (uint32_t)&core1_image_start;
                 75
                 76
                                  return core1_image_size;
                 77
                 78
                         #endif
                  79⊕ /*!
                           * @brief Main function
                 81
                 82@ int main(void)
                 83
                        {
                                   /* Define the init structure for the switches*/
                 gpio_pin_config_t sw_config = {kGPIO_DigitalInput, 0};
                 86
                  87
                                   /* Init board hardware.*/
                                   /* attach 12 MHz clock to FLEXCOMM0 (debug console) */
                  88
                                  CLOCK_AttachClk(kFR012M_to_FLEXCOMM0);
                  90
                                  BOARD_InitPins_Core0();
                 91
                                  BOARD_BootClockFROHF48M();
                  92
                 93
                                  BOARD_InitDebugConsole();
                  95
                                   /* Init switches */
                                  GPIO PinInit(BOARD SW1 GPIO, BOARD SW1 GPIO PORT, BOARD SW1 GPIO PIN, &sw config);
                  96
                                  GPIO_PinInit(BOARD_SW2_GPIO, BOARD_SW2_GPIO_PORT, BOARD_SW2_GPIO_PIN, &sw_config);
                  97
```

Now, the two debug sessions should be opened, and the debug controls can be used for both debug sessions depending on the debug session selection. Keep the primary core debug session selected by clicking the "Resume" button. The hello\_world multicore application then starts running. The primary core application starts the auxiliary core application during runtime, and the auxiliary core application stops at the beginning of the main() function. The debug session of the auxiliary core application is highlighted. After clicking the "Resume" button, it is applied to the auxiliary core debug session. Therefore, the auxiliary core application continues its execution.

```
📈 workspace - Develop - Ipcxpresso54114_multicore_examples_hello_world_cm0plus/source/hello_world_core1.c - MCUXpresso IDE
File Edit Source Refactor Navigate Search Project Run FreeRTOS Window Help
▼ 🗗 ▼ 🕡 ▼ 🐉 🕻 📞 🐉 🛷 🎉 🗿 🗊 🐗 🖟 🖟 🖟 🖟 🖟 🔝 🖜 ▼ 🏈 🖟 🔞 😭 🔐 😭
                                                                                       Step Return All Debug sessions

★ Debug 

□

      ▲ X Ipcxpresso54114_multicore_examples_hello_world_cm4 Debug [C/C++ (NXP Semiconductors) MCU Application]
6
         Ipcxpresso54114_multicore_examples_hello_world_cm4.axf [LPC54114J256 (cortex-m0plus)]
 굶
              Thread #11 (Stopped) (Running)
1010
0101
           arm-none-eabi-gdb (7.12.0.20161204)
*

■ Ipcxpresso54114_multicore_examples_hello_world_cm0plus Debug [C/C++ (NXP Semiconductors) MCU Application]

         ■ Ipcxpresso54114_multicore_examples_hello_world_cm0plus.axf [LPC54114J256 (cortex-m0plus)]
            8
                main() at hello_world_core1.c:71 0x20010846
 (1)
           arm-none-eabi-gdb (7.12.0.20161204)
(x)=
(x)=
00
믊
                                            nello_world_core1.c ⊠
      hello_world_core0.c
                         .h fsl_mailbox.h
                }
        61 }
        62
        63⊕ /*!
        64 * @brief Main function
65 */
        65
        66⊖ int main(void)
        67 {
                uint32_t startupData, i;
        68
        69
                /* Define the init structure for the output LED pin*/
        70
                gpio_pin_config_t led_config = {
        71
        72
                    kGPIO DigitalOutput, 0,
        73
        74
        75
                /* Initialize MCMGR before calling its API */
        76
               MCMGR_Init();
        77
                /* Get the startup data */
        78
               MCMGR_GetStartupData(kMCMGR_Core1, &startupData);
        79
        80
        81
                /* Make a noticable delay after the reset */
                /* Use startup parameter from the master core... */
        82
        83
                for (i = 0; i < startupData; i++)</pre>
        84
                    delay();
```

At this point, it is possible to suspend and resume individual cores independently. It is also possible to make synchronous suspension and resumption of both the cores. This is done either by selecting both opened debug sessions (multiple selections) and clicking the "Suspend" / "Resume" control button, or just using the "Suspend All Debug sessions" and the "Resume All Debug sessions" buttons.

```
💢 workspace - Develop - lpcxpresso54114_multicore_examples_hello_world_cm0plus/source/hello_world_core1.c - MCUXpresso IDE
<u>File Edit Source Refactor Navigate Search Project Run FreeRTOS Window Help</u>
                                          ▼ 🔾 ▼ 🐉 🖟 🦠 🐉 🕬 🚅 🛍 🐠 🕷 🔯 🗗 🛊 ▼ 🔾 🔻

■ Ipcxpresso54114_multicore_examples_hello_world_cm4 Debug [C/C++ (NXP Semiconductors) MCU Application]

6

■ ipcxpresso54114_multicore_examples_hello_world_cm4.axf [LPC54114J256 (cortex-m0plus)]

 몲
              Thread #1 1 (Stopped) (Running)
 1010
0101
            arm-none-eabi-gdb (7.12.0.20161204)
 *

■ Ipcxpresso54114_multicore_examples_hello_world_cm0plus Debug [C/C++ (NXP Semiconductors) MCU Application]

         Ipcxpresso54114_multicore_examples_hello_world_cm0plus.axf [LPC54114J256 (cortex-m0plus)]
              Thread #1 1 (Stopped) (Running)
 æ
           arm-none-eabi-gdb (7.12.0.20161204)
 ம
(x)=
(x)=
 0
 먎
      .c hello_world_core0.c
                             h fsl_mailbox.h c hello_world_core1.c ⋈ c 0x190
                      asm("NOP"); /* delay */
        60
        61 }
        62
        63⊕ /*!
        64 * @brief Main function
65 */
        66⊖ int main(void)
        67 {
        68
                uint32_t startupData, i;
        69
                /* Define the <u>init</u> structure for the output LED pin*/
        70
        71
                gpio_pin_config_t led_config = {
        72
                    kGPIO_DigitalOutput, 0,
        73
        74
                /* Initialize MCMGR before calling its API */
        75
        76
                MCMGR_Init();
        77
        78
                /* Get the startup data */
        79
                MCMGR_GetStartupData(kMCMGR_Core1, &startupData);
        80
        81
                /* Make a noticable delay after the reset */
                /* Use startup parameter from the master core... */
        82
        83
                for (i = 0; i < startupData; i++)</pre>
        84
                    delay();
```

```
📈 workspace - Develop - Ipcxpresso54114_multicore_examples_hello_world_cm0plus/source/hello_world_core1.c - MCUXpresso IDE
<u>File Edit Source Refactor Navigate Search Project Run FreeRTOS Window Help</u>
 8

■ Ipcxpresso54114_multicore_examples_hello_world_cm4 Debug [C/C++ (NXP Semiconductors) MCU Application]

6

■ ipcxpresso54114_multicore_examples_hello_world_cm4.axf [LPC54114J256 (cortex-m0plus)]

 몲
            Thread #1 1 (Stopped) (Suspended : Signal : SIGINT:Interrupt)
 1010
0101
                 GPIO_ReadPinInput() at fsl_gpio.h:146 0x95c
 *
                 main() at hello_world_core0.c:134 0xa10
            arm-none-eabi-gdb (7.12.0.20161204)
 Ð

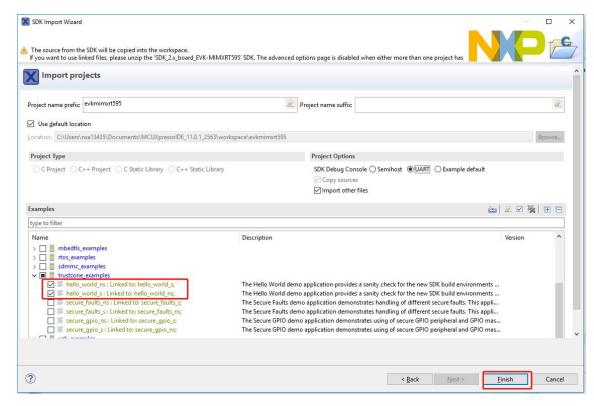
■ MI lpcxpresso54114_multicore_examples_hello_world_cm0plus Debug [C/C++ (NXP Semiconductors) MCU Application]

■ Ipcxpresso54114_multicore_examples_hello_world_cm0plus.axf [LPC54114J256 (cortex-m0plus)]

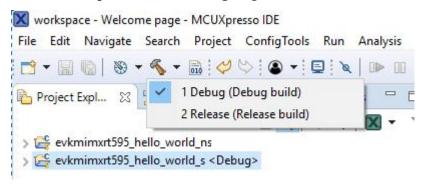
 ψ
            Thread #1 1 (Stopped) (Suspended: Signal: SIGINT:Interrupt)
(x)=
                 delay() at hello_world_core1.c:59 0x20010824
(x)=
                 main() at hello_world_core1.c:99 0x200108a0
 0
           arm-none-eabi-gdb (7.12.0.20161204)
 믊
      hello_world_core0.c
                            .h fsl_mailbox.h
                                              le hello_world_core1.c ⋈ le 0x190
        59
                      asm("NOP"); /* delay */
        60
        61 }
        62
        63@ /*!
            * @brief Main function
        660 int main(void)
        67 {
        68
                uint32_t startupData, i;
        70
                /* Define the init structure for the output LED pin*/
                gpio_pin_config_t led_config = {
        71
        72
                    kGPIO_DigitalOutput, 0,
        73
        74
        75
                /* Initialize MCMGR before calling its API */
        76
                MCMGR_Init();
        77
        78
                /* Get the startup data */
        79
                MCMGR_GetStartupData(kMCMGR_Core1, &startupData);
        80
                /* Make a noticable delay after the reset */
        81
        82
                /* Use startup parameter from the master core... */
        83
                for (i = 0; i < startupData; i++)
                    delay();
```

**Build a TrustZone example application** This section describes the steps required to configure MCUXpresso IDE to build, run, and debug TrustZone example applications. The TrustZone version of the hello\_world example application targeted for the MIMXRT595-EVK hardware platform is used as an example, though these steps can be applied to any TrustZone example application in the MCUXpresso SDK.

- 1. TrustZone examples are imported into the workspace in a similar way as single core applications. When the SDK zip package for MIMXRT595-EVK is installed and available in the Installed SDKs view, click Import SDK example(s)... on the Quickstart Panel. In the window that appears, expand the MIMXRT500 folder and select MIMXRT595S. Then, select evkmimxrt595 and click Next.
- 2. Expand the trustzone\_examples/ folder and select hello\_world\_s. Because TrustZone examples are linked together, the non-secure project is automatically imported with the secure project, and there is no need to select it explicitly. Then, click **Finish**.

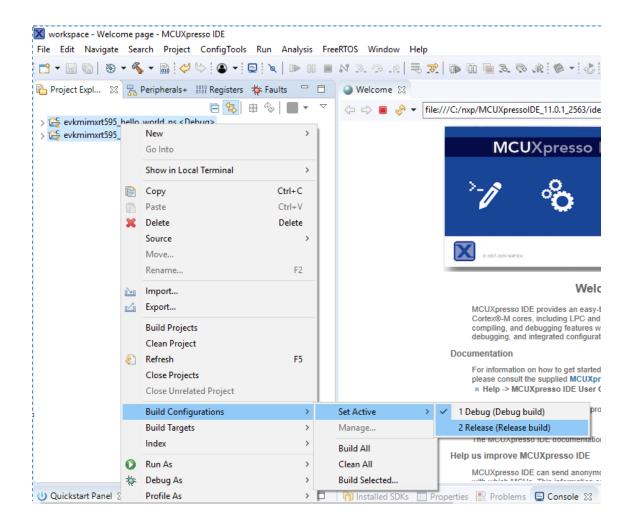


3. Now, two projects should be imported into the workspace. To start building the TrustZone application, highlight the <code>evkmimxrt595\_hello\_world\_s</code> project (TrustZone master project) in the Project Explorer. Then, choose the appropriate build target, **Debug** or **Release**, by clicking the downward facing arrow next to the hammer icon, as shown in following figure. For this example, select the **Debug** target.

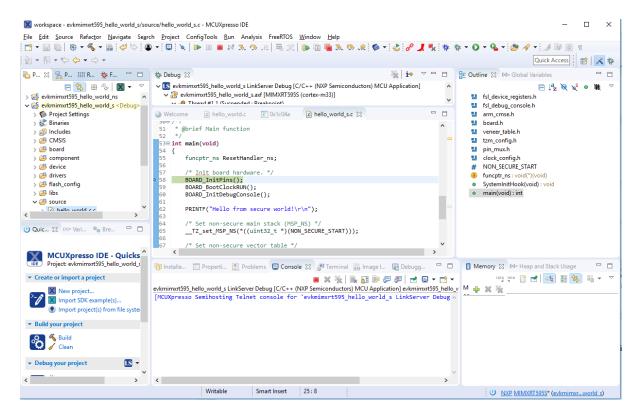


The project starts building after the build target is selected. It is requested to build the application for the secure project first, because the non-secure project must know the secure project since CMSE library when running the linker. It is not possible to finish the non-secure project linker when the secure project since CMSE library is not ready.

**Note:** When the **Release** build is requested, it is necessary to change the build configuration of both the secure and non-secure application projects first. To do this, select both projects in the Project Explorer view by clicking to select the first project, then using shift-click or control-click to select the second project. Right click in the Project Explorer view to display the context-sensitive menu and select **Build Configurations** > **Set Active** > **Release**. This is also possible by using the menu item of **Project** > **Build Configuration** > **Set Active** > **Release**. After switching to the **Release** build configuration. Build the application for the secure project first.



**Run a TrustZone example application** To download and run the application, perform all steps as described in **Run an example application**. These steps are common for single core, and TrustZone applications, ensuring <br/>
<br/>
| board\_name > \_hello\_world\_s is selected for debugging. In the Quickstart Panel, click **Debug** to launch the second debug session.



Now, the TrustZone sessions should be opened. Click **Resume**. The hello\_world TrustZone application then starts running, and the secure application starts the non-secure application during runtime.

#### Run a demo application using IAR

This section describes the steps required to build, run, and debug example applications provided in the MCUXpresso SDK.

**Note:** IAR Embedded Workbench for Arm version 8.32.3 is used in the following example, and the IAR toolchain should correspond to the latest supported version, as described in the *MCUX-presso SDK Release Notes*.

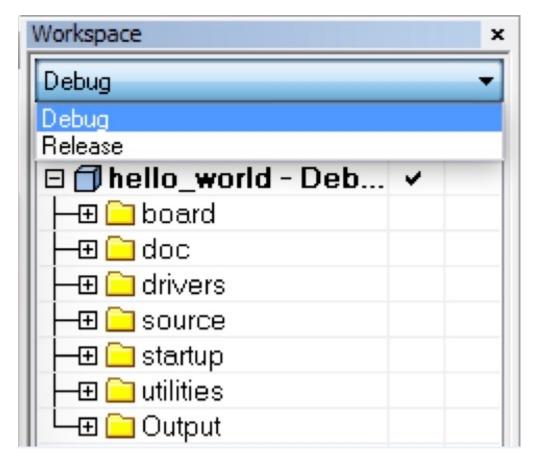
**Build an example application** Do the following steps to build the hello\_world example application.

1. Open the desired demo application workspace. Most example application workspace files can be located using the following path:

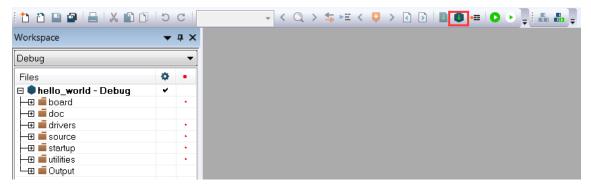
Other example applications may have additional folders in their path.

2. Select the desired build target from the drop-down menu.

For this example, select hello\_world - debug.



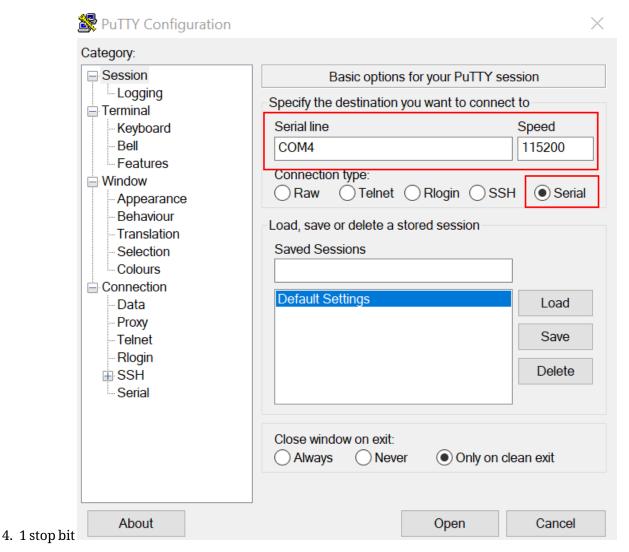
3. To build the demo application, click Make, highlighted in red in following figure.



4. The build completes without errors.

**Run an example application** To download and run the application, perform these steps:

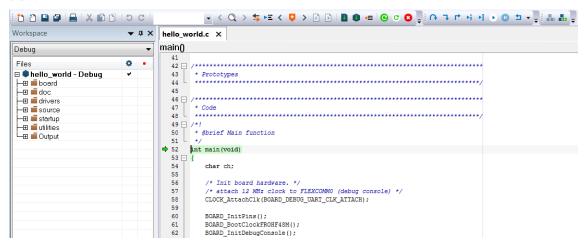
- 1. Ensure the host driver for the debugger firmware has been installed. See *On-board debugger*.
- 2. Connect the development platform to your PC via USB cable.
- 3. Open the terminal application on the PC, such as PuTTY or TeraTerm, and connect to the debug COM port (to determine the COM port number, see *How to determine COM port*). Configure the terminal with these settings:
  - 1. 115200 or 9600 baud rate, depending on your board (reference BOARD\_DEBUG\_UART\_BAUDRATE variable in the board.h file)
  - 2. No parity
  - 3. 8 data bits



4. In IAR, click the **Download and Debug** button to download the application to the target.



5. The application is then downloaded to the target and automatically runs to the  $\min()$  function.



6. Run the code by clicking the **Go** button.



7. The hello\_world application is now running and a banner is displayed on the terminal. If it does not appear, check your terminal settings and connections.



**Build a multicore example application** This section describes the steps to build and run a dual-core application. The demo applications workspace files are located in this folder:

Begin with a simple dual-core version of the Hello World application. The multicore Hello World IAR workspaces are located in this folder:

Build both applications separately by clicking the **Make** button. Build the application for the auxiliary core (cm0plus) first, because the primary core application project (cm4) must know the auxiliary core application binary when running the linker. It is not possible to finish the primary core linker when the auxiliary core application binary is not ready.

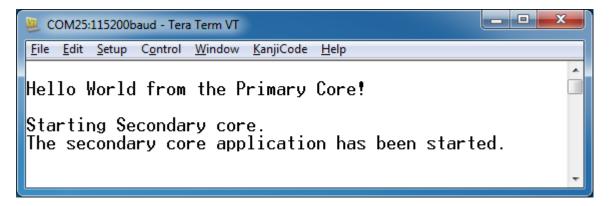
**Run a multicore example application** The primary core debugger handles flashing both primary and the auxiliary core applications into the SoC flash memory. To download and run the multicore application, switch to the primary core application project and perform steps 1-4 as described in **Run an example application**. These steps are common for both single core and dual-core applications in IAR.

After clicking the "Download and Debug" button, the auxiliary core project is opened in the separate EWARM instance. Both the primary and auxiliary images are loaded into the device flash memory and the primary core application is executed. It stops at the default C language entry point in the \*main()\*function.

Run both cores by clicking the "Start all cores" button to start the multicore application.



During the primary core code execution, the auxiliary core is released from the reset. The hello\_world multicore application is now running and a banner is displayed on the terminal. If this does not appear, check the terminal settings and connections.



An LED controlled by the auxiliary core starts flashing, indicating that the auxiliary core has been released from the reset and is running correctly. When both cores are running, use the "Stop all cores", and "Start all cores" control buttons to stop or run both cores simultaneously.



**Build a TrustZone example application** This section describes the particular steps that must be done in order to build and run a TrustZone application. The demo applications workspace files are located in this folder:

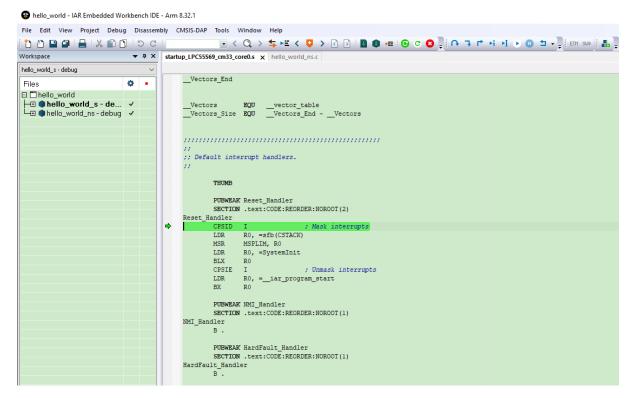
```
 $$ < install\_dir > boards / coard\_name > /trustzone\_examples / capplication\_name > /[core\_type >]/iar / capplication\_name > _ns/iar $$ $$ < install\_dir > /boards / coard\_name > /trustzone\_examples / capplication\_name > /[core\_type >]/iar / capplication\_name > _s/iar $$ $$ < application\_name > _s/iar $$ < application\_name > _s/i
```

Begin with a simple TrustZone version of the Hello World application. The TrustZone Hello World IAR workspaces are located in this folder:

```
 < install\_dir > /boards / < board\_name > /trustzone\_examples / hello\_world / hello\_world\_ns / iar / hello\_world\_world\_world\_s. \\ < install\_dir > /boards / < board\_name > /trustzone\_examples / hello\_world / hello\_world\_s / iar / hello\_world\_s. \\ < install\_dir > /boards / < board\_name > /trustzone\_examples / hello\_world / hello\_world\_s / iar / hello\_world.eww
```

This project hello\_world.eww contains both secure and non-secure projects in one workspace and it allows the user to easily transition from one project to another. Build both applications separately by clicking **Make**. It is requested to build the application for the secure project first, because the non-secure project must know the secure project, since the CMSE library is running the linker. It is not possible to finish the non-secure project linker with the secure project since CMSE library is not ready.

Run a TrustZone example application The secure project is configured to download both secure and non-secure output files, so debugging can be fully managed from the secure project. To download and run the TrustZone application, switch to the secure application project and perform steps 1-4 as described in Run an example application. These steps are common for both single core, and TrustZone applications in IAR. After clicking **Download and Debug**, both the secure and non-secure images are loaded into the device memory, and the secure application is executed. It stops at the Reset\_Handler function.



Run the code by clicking **Go** to start the application.

The TrustZone hello\_world application is now running and a banner is displayed on the terminal. If this is not true, check your terminal settings and connections.

```
COM57-PuTTY — X

Hello from secure world!

Entering normal world.

Welcome in normal world!

This is a text printed from normal world!

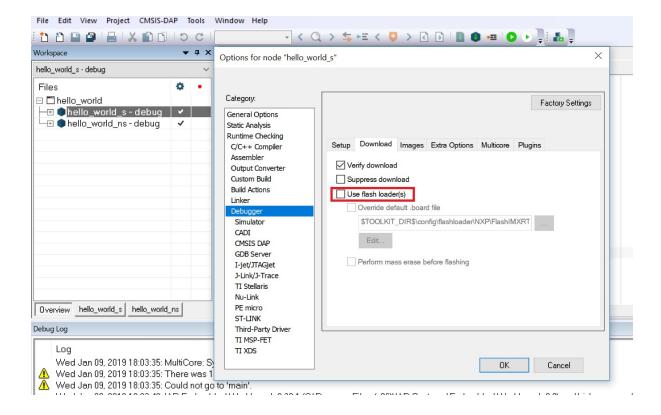
Comparing two string as a callback to normal world

String 1: Test1

String 2: Test2

Both strings are not equal!
```

**Note:** If the application is running in RAM (debug/release build target), in **Options\*\*>\*\*Debugger > Download** tab, disable **Use flash loader(s)**. This can avoid the \_ns download issue on i.MXRT500.



#### Run a demo using Keil MDK/µVision

This section describes the steps required to build, run, and debug example applications provided in the MCUXpresso SDK.

**Install CMSIS device pack** After the MDK tools are installed, Cortex Microcontroller Software Interface Standard (CMSIS) device packs must be installed to fully support the device from a debug perspective. These packs include things such as memory map information, register definitions, and flash programming algorithms. Follow these steps to install the appropriate CMSIS pack.

1. Open the MDK IDE, which is called  $\mu$ Vision. In the IDE, select the **Pack Installer** icon.



2. After the installation finishes, close the Pack Installer window and return to the  $\mu Vision$  IDE.

#### Build an example application

1. Open the desired example application workspace in:

The workspace file is named as <demo\_name>.uvmpw. For this specific example, the actual path is:

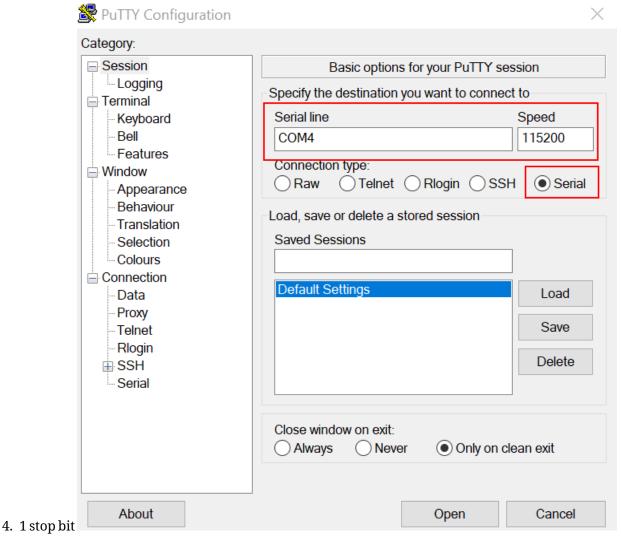
2. To build the demo project, select **Rebuild**, highlighted in red.



3. The build completes without errors.

**Run an example application** To download and run the application, perform these steps:

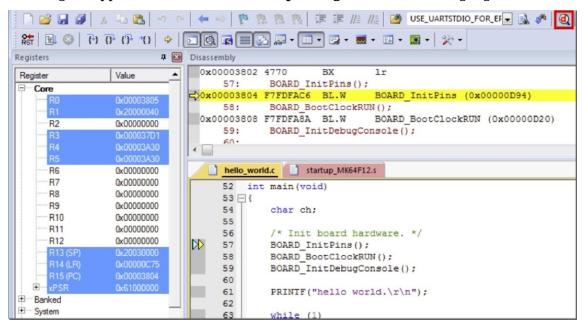
- 1. Ensure the host driver for the debugger firmware has been installed. See *On-board debugger*.
- 2. Connect the development platform to your PC via USB cable using USB connector.
- 3. Open the terminal application on the PC, such as PuTTY or TeraTerm and connect to the debug serial port number (to determine the COM port number, see *How to determine COM port*. Configure the terminal with these settings:
  - 1. 115200 or 9600 baud rate, depending on your board (reference BOARD\_DEBUG\_UART\_BAUDRATE variable in the board.h file)
  - 2. No parity
  - 3. 8 data bits



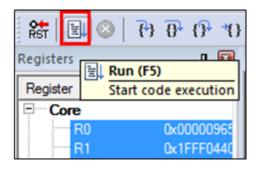
4. In  $\mu$ Vision, after the application is built, click the **Download** button to download the application to the target.



5. After clicking the **Download** button, the application downloads to the target and is running. To debug the application, click the **Start/Stop Debug Session** button, highlighted in red.



6. Run the code by clicking the **Run** button to start the application.



The hello\_world application is now running and a banner is displayed on the terminal. If this does not appear, check your terminal settings and connections.



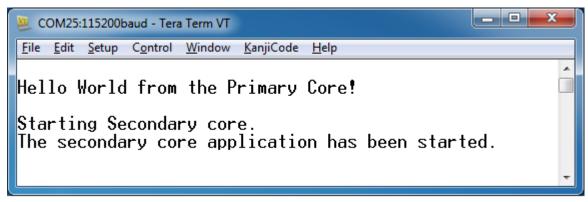
**Build a multicore example application** This section describes the steps to build and run a dual-core application. The demo applications workspace files are located in this folder:

Begin with a simple dual-core version of the Hello World application. The multicore Hello World Keil MSDK/µVision workspaces are located in this folder:

Build both applications separately by clicking the **Rebuild** button. Build the application for the auxiliary core (cm0plus) first because the primary core application project (cm4) must know the auxiliary core application binary when running the linker. It is not possible to finish the primary core linker when the auxiliary core application binary is not ready.

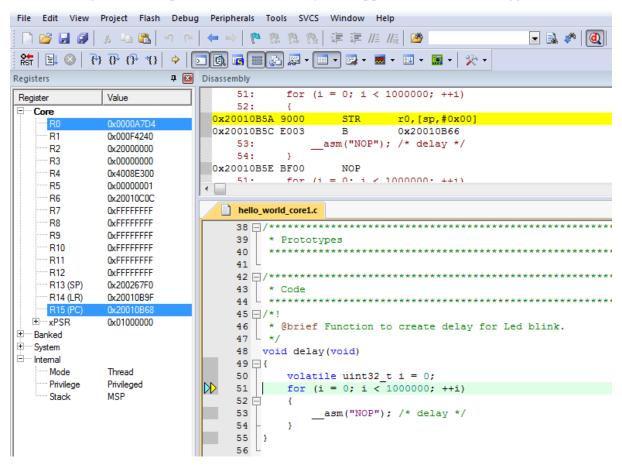
Run a multicore example application The primary core debugger flashes both the primary and the auxiliary core applications into the SoC flash memory. To download and run the multicore application, switch to the primary core application project and perform steps 1-5 as described in Run an example application. These steps are common for both single-core and dual-core applications in  $\mu$ Vision.

Both the primary and the auxiliary image is loaded into the device flash memory. After clicking the "Run" button, the primary core application is executed. During the primary core code execution, the auxiliary core is released from the reset. The hello\_world multicore application is now running and a banner is displayed on the terminal. If this does not appear, check your terminal settings and connections.



An LED controlled by the auxiliary core starts flashing indicating that the auxiliary core has been released from the reset and is running correctly.

Attach the running application of the auxiliary core by opening the auxiliary core project in the second  $\mu$ Vision instance and clicking the "Start/Stop Debug Session" button. After this, the second debug session is opened and the auxiliary core application can be debugged.



Arm describes multicore debugging using the NXP LPC54114 Cortex-M4/M0+ dual-core processor and Keil uVision IDE in Application Note 318 at www.keil.com/appnotes/docs/apnt\_318.asp. The associated video can be found here.

**Build a TrustZone example application** This section describes the particular steps that must be done in order to build and run a TrustZone application. The demo applications workspace files are located in this folder:

Begin with a simple TrustZone version of the Hello World application. The TrustZone Hello World Keil MSDK/ $\mu$ Vision workspaces are located in this folder:

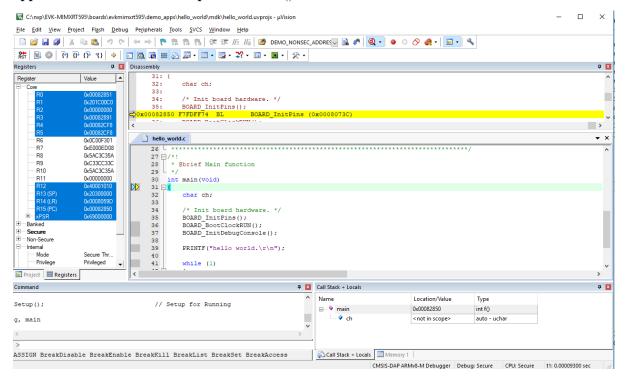
```
\label{lowerld_world_world} $$ < \frac{dir}{boards} < \frac{name}{trustzone} = \frac{examples}{hello} \frac{dir}{hello} \frac{s}{mdk} / \frac{hello}{world}. $$
```

This project hello\_world.uvmpw contains both secure and non-secure projects in one workspace and it allows the user to easily transition from one project to another.

Build both applications separately by clicking **Rebuild**. It is requested to build the application for the secure project first, because the non-secure project must know the secure project since CMSE library is running the linker. It is not possible to finish the non-secure project linker with the secure project because CMSE library is not ready.

**Run a TrustZone example application** The secure project is configured to download both secure and non-secure output files so debugging can be fully managed from the secure project.

To download and run the TrustZone application, switch to the secure application project and perform steps as described in **Run an example application**. These steps are common for single core, dual-core, and TrustZone applications in  $\mu$ Vision. After clicking **Download and Debug**, both the secure and non-secure images are loaded into the device flash memory, and the secure application is executed. It stops at the  $\min()$  function.



Run the code by clicking **Run** to start the application.

The hello\_world application is now running and a banner is displayed on the terminal. If not, check your terminal settings and connections.

```
COM57-PuTTY — X

Hello from secure world!

Entering normal world.

Welcome in normal world!

This is a text printed from normal world!

Comparing two string as a callback to normal world

String 1: Test1

String 2: Test2

Both strings are not equal!
```

## Run a demo using Arm GCC

This section describes the steps to configure the command-line Arm GCC tools to build, run, and debug demo applications and necessary driver libraries provided in the MCUXpresso SDK. The hello world demo application is targeted which is used as an example.

**Set up toolchain** This section contains the steps to install the necessary components required to build and run an MCUXpresso SDK demo application with the Arm GCC toolchain, as supported by the MCUXpresso SDK. There are many ways to use Arm GCC tools, but this example focuses on a Windows operating system environment.

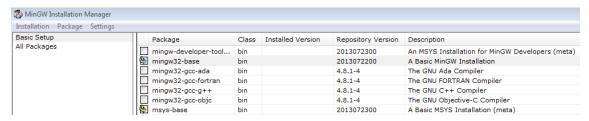
**Install GCC Arm Embedded tool chain** Download and run the installer from GNU Arm Embedded Toolchain. This is the actual toolset (in other words, compiler, linker, and so on). The GCC toolchain should correspond to the latest supported version, as described in **MCUXpresso SDK Release Notes**.

**Install MinGW (only required on Windows OS)** The Minimalist GNU for Windows (MinGW) development tools provide a set of tools that are not dependent on third-party C-Runtime DLLs (such as Cygwin). The build environment used by the MCUXpresso SDK does not use the MinGW build tools, but does leverage the base install of both MinGW and MSYS. MSYS provides a basic shell with a Unix-like interface and tools.

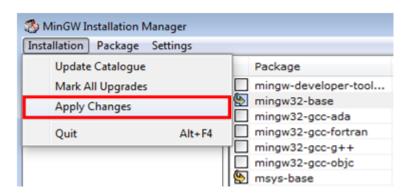
- 1. Download the latest MinGW mingw-get-setup installer from MinGW.
- 2. Run the installer. The recommended installation path is  $C:\MinGW$ , however, you may install to any location.

**Note:** The installation path cannot contain any spaces.

3. Ensure that the **mingw32-base** and **msys-base** are selected under **Basic Setup**.



4. In the **Installation** menu, click **Apply Changes** and follow the remaining instructions to complete the installation.

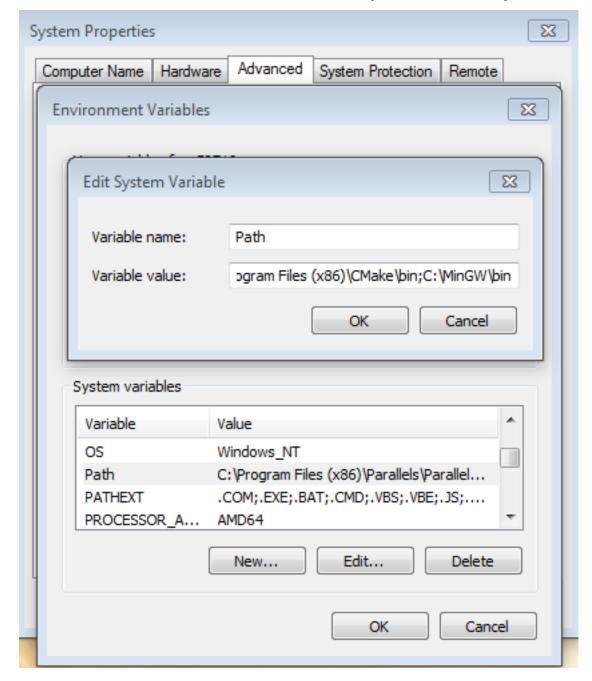


5. Add the appropriate item to the Windows operating system path environment variable. It can be found under **Control Panel->System and Security->System->Advanced System Settings** in the **Environment Variables...** section. The path is:

<mingw\_install\_dir>\bin

Assuming the default installation path, C:\MinGW, an example is shown below. If the path is not set correctly, the toolchain will not work.

**Note:** If you have  $C:\min GW\setminus msys\setminus x.x\setminus bin$  in your PATH variable (as required by Kinetis SDK 1.0.0), remove it to ensure that the new GCC build system works correctly.

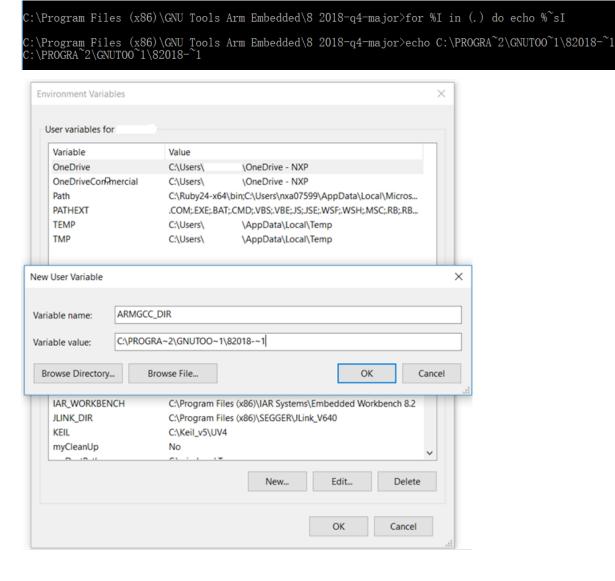


**Add a new system environment variable for ARMGCC\_DIR** Create a new *system* environment variable and name it as ARMGCC\_DIR. The value of this variable should point to the Arm GCC Embedded tool chain installation path. For this example, the path is:

C:\Program Files (x86)\GNU Tools Arm Embedded\8 2018-q4-major

See the installation folder of the GNU Arm GCC Embedded tools for the exact pathname of your installation.

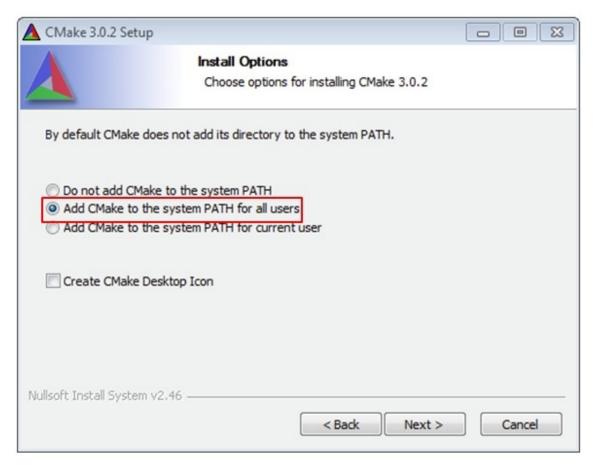
Short path should be used for path setting, you could convert the path to short path by running command for %I in (.) do echo %-\$I in above path.



### **Install CMake**

## Windows OS

- 1. Download CMake 3.0.x from www.cmake.org/cmake/resources/software.html.
- 2. Install CMake, ensuring that the option **Add CMake to system PATH** is selected when installing. The user chooses to select whether it is installed into the PATH for all users or just the current user. In this example, it is installed for all users.



- 3. Follow the remaining instructions of the installer.
- 4. You may need to reboot your system for the PATH changes to take effect.
- 5. Make sure sh.exe is not in the Environment Variable PATH. This is a limitation of mingw32-make.

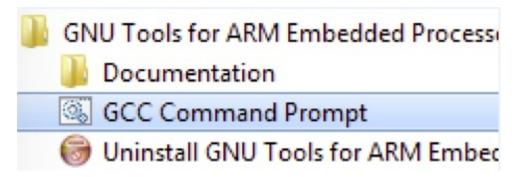
**Linux OS** It depends on the distributions of Linux Operation System. Here we use Ubuntu as an example.

Open shell and use following commands to install cmake and its version. Ensure the cmake version is above 3.0.x.

```
$ sudo apt-get install cmake
$ cmake --version
```

**Build an example application** To build an example application, follow these steps.

 Open a GCC Arm Embedded tool chain command window. To launch the window, from the Windows operating system Start menu, go to Programs >GNU Tools Arm Embedded <version> and select GCC Command Prompt.



2. Change the directory to the example application project directory which has a path similar to the following:

For this example, the exact path is:

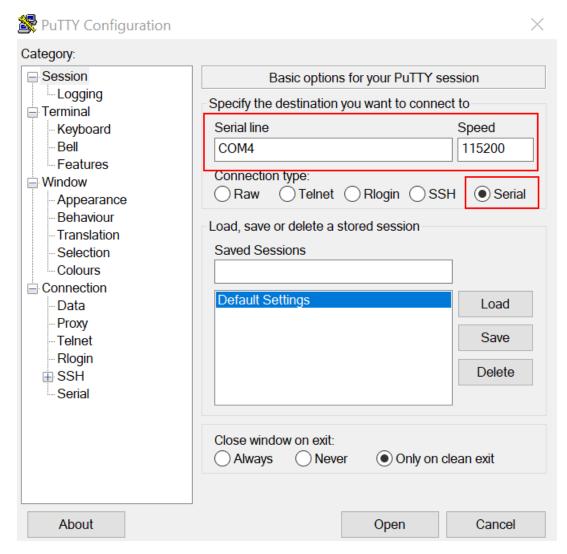
**Note:** To change directories, use the cd command.

3. Type **build\_debug.bat** on the command line or double click on **build\_debug.bat** file in Windows Explorer to build it. The output is as shown in following figure.

**Run an example application** This section describes steps to run a demo application using J-Link GDB Server application. To install J-Link host driver and update the on-board debugger firmware to Jlink firmware, see *On-board debugger*.

After the J-Link interface is configured and connected, follow these steps to download and run the demo applications:

- 1. Connect the development platform to your PC via USB cable between the on-board debugger USB connector and the PC USB connector. If using a standalone J-Link debug pod, connect it to the SWD/JTAG connector of the board.
- 2. Open the terminal application on the PC, such as PuTTY or TeraTerm, and connect to the debug serial port number (to determine the COM port number, see *How to determine COM port*). Configure the terminal with these settings:
  - 1. 115200 or 9600 baud rate, depending on your board (reference BOARD\_DEBUG\_UART\_BAUDRATE variable in board.h file)
  - 2. No parity
  - 3. 8 data bits
  - 4. 1 stop bit

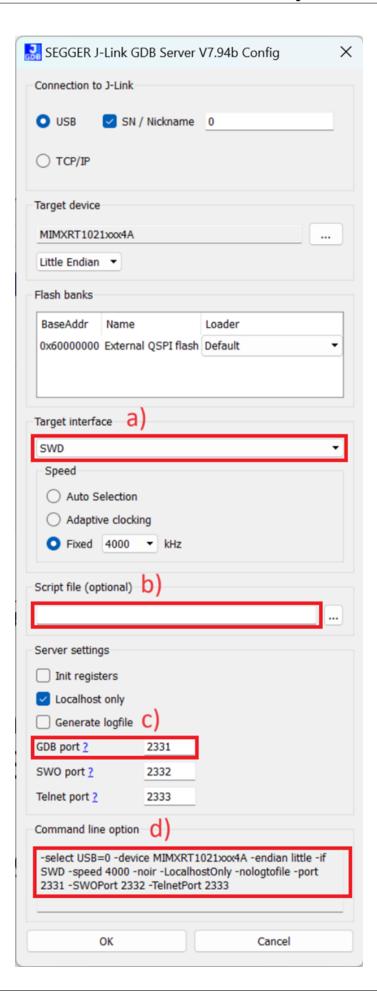


3. To launch the application, open the Windows **Start** menu and select **Programs > SEGGER** > **J-Link <version> J-Link GDB Server**.

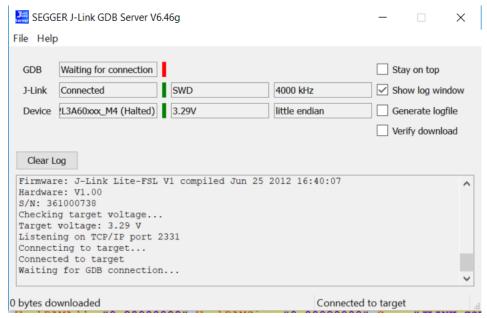
**Note:** It is assumed that the J-Link software is already installed.

The **SEGGER J-Link GDB Server Config** settings dialog appears.

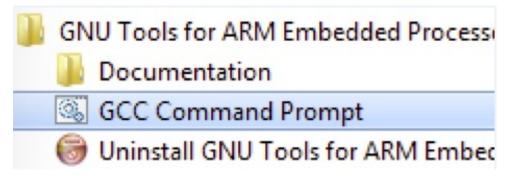
- 4. Make sure to check the following options.
  - 1. **Target interface**: The debug connection on board uses internal SWD signaling. In case of a wrong setting J-Link is unable to communicate with device under test.
  - 2. **Script file**: If required, a J-Link init script file can be used for board initialization. The file with the ".jlinkscript" file extension is located in the <install\_dir>/boards/<br/><box/board name>/ directory.
  - 3. Under the **Server settings**, check the GDB port for connection with the gdb target remote command. For more information, see step 9.
  - 4. There is a command line version of J-Link GDB server "JLinkGDBServerCL.exe". Typical path is C:\Program Files\SEGGER\JLink\. To start the J-Link GDB server with the same settings as are selected in the UI, you can use these command line options.



5. After it is connected, the screen should look like this figure:



6. If not already running, open a GCC Arm Embedded tool chain command window. To launch the window, from the Windows operating system Start menu, go to **Programs - GNU Tools Arm Embedded <version>** and select **GCC Command Prompt**.



7. Change to the directory that contains the example application output. The output can be found in using one of these paths, depending on the build target selected:

```
\label{lem:constall_dir} $$ \left(\frac{\sin tall_dir}{boards} \right) = \frac{\cot u}{\cot u} - \frac{\cot u}{\cot u} -
```

8. Run the arm-none-eabi-gdb.exe <application\_name>.elf command. For this example, it is arm-none-eabi-gdb.exe hello\_world.elf.

```
C:\Program Files (x86)\GNU Tools ARM Embedded\8 2018-q4-major>arm-none-eabi-gdb.exe C:\Users\nxa12829\Desktop\k3213\boards\frdmk32l3a6\demo_apps\hello_world\cm4\armgcc\debug\hello_world\cm4\armgcc\debug\hello_world\demo_cm4.elf
C:\Program Files (x86)\GNU Tools ARM Embedded\8 2018-q4-major>arm-none-eabi-gdb.exe: warning: Couldn't determine a path for the index cache directory.
GNU gdb (GNU Tools for Arm Embedded Processors 8-2018-q4-major) 8.2.50.20181213-git
Copyright (C) 2018 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later \http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.
Type "show copying" and "show warranty" for details.
This GDB was configured as "--host=i686-w64-mingw32 --target=arm-none-eabi".
Type "show configuration" for configuration details.
For bug reporting instructions, please see:
\http://www.gnu.org/software/gdb/bugs/>.
Find the GDB manual and other documentation resources online at:
\http://www.gnu.org/software/gdb/documentation/>.

For help, type "help".
Type "apropos word" to search for commands related to "word"...
Reading symbols from C:\Users\nxa12829\Desktop\k3213\boards\frdmk3213a6\demo_apps\hello_world\cm4\armgcc\debug\hello_world
ddemo_cm4.elf...
(gdb)
```

- 9. Run these commands:
  - 1. target remote localhost:2331
  - 2. monitor reset
  - 3. monitor halt
  - 4. load
  - 5. monitor reset
- 10. The application is now downloaded and halted. Execute the  ${
  m monitor}\ {
  m go}\ command$  to start the demo application.

The hello\_world application is now running and a banner is displayed on the terminal. If this does not appear, check your terminal settings and connections.



**Build a multicore example application** This section describes the steps to build and run a dual-core application. The demo application build scripts are located in this folder:

Begin with a simple dual-core version of the Hello World application. The multicore Hello World GCC build scripts are located in this folder:

```
< install\_dir > /boards/lpcxpresso 54114/multicore\_examples/hello\_world/cm0plus/armgcc/build\_debug.bat \\ < install\_dir > /boards/lpcxpresso 54114/multicore\_examples/hello\_world/cm4/armgcc/build\_debug.bat \\
```

Build both applications separately following steps for single core examples as described in **Build** an example application.

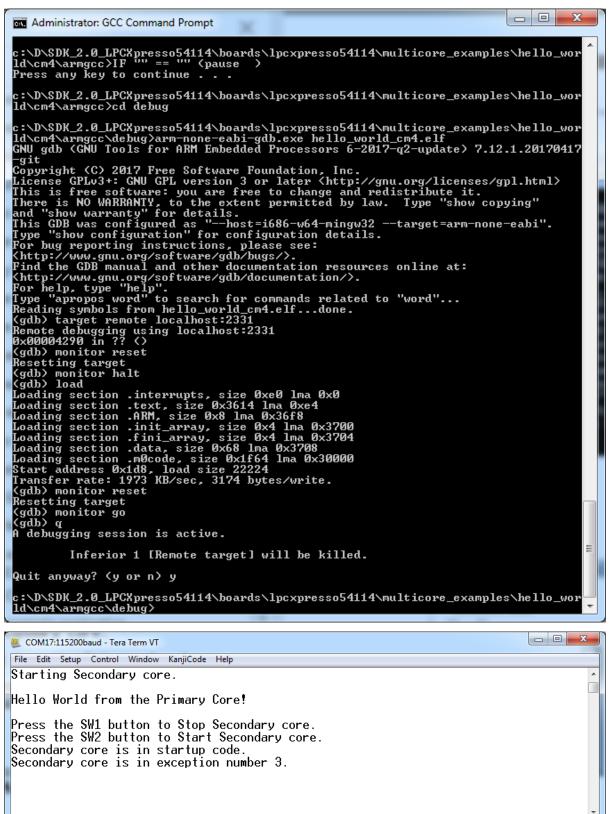
```
GCC Command Prompt - build_debug.bat
 52%]
           debug_console/fsl_debug_console.c.obj
lding_C_object_CMakeFiles/hello_world_cm0plus.elf.dir/C_/packages/SDK_2.6.0_FRDM-K32L3A6_RC1/devices/K32L3A60
 69%1
                 manager.c.ouj
C object CMakeFiles/hello_world_cm0plus.elf.dir/C_/packages/SDK 2.6.0 FRDM-K32L3A6 RC1/comp
                   ort_uart.c.obj
object CMakeFiles/hello world cm0plus.elf.dir/C /packages/SDK 2.6.0 FRDM-K32L3A6 RC1/0
 82%]
 86%]
100%] Built target hello_world_cm0plus.elf
::\packages\SDK 2.6.0 FRDM-K32L3A6 RC1\boards\frdmk32l3a6\multicore examples\hello world\cm0plus\armgcc>IF "" == "" (pa
     any key to continue
GCC Command Prompt - build debug.bat
 58%1
 62%1
 70%1
          ug_console/fsl_debug_console.c.obj
ilding C_object_CMakeFiles/hello_world_cm4.elf.dir/C_/packages/SDK_2.6.0_FRDM-K32L3A6_RC1/c
       Building ASM object CMakeFiles/hello_world_cm4.elf.dir/C_/packages/SDK 2.6.0 FRDM-K32L3A6 RC1/devices/K32L3A60/s
 95%]
190%] Linking C executable debug\hello_world_cm4.elf
190%] Built target hello_world_cm4.elf
:\packages\SDK_2.6.0_FRDM-K32L3A6_RC1\boards\frdmk32l3a6\multicore_examples\hello_world\cm4\armgcc>IF "" == "" (pause
```

**Run a multicore example application** When running a multicore application, the same prerequisites for J-Link/J-Link OpenSDA firmware, and the serial console as for the single-core application, applies, as described in **Run an example application**.

The primary core debugger handles flashing of both the primary and the auxiliary core applications into the SoC flash memory. To download and run the multicore application, switch to the primary core application project and perform steps 1 to 10, as described in **Run an example application**. These steps are common for both single-core and dual-core applications in Arm GCC.

Both the primary and the auxiliary image is loaded into the SPI flash memory. After execution of the monitor go command, the primary core application is executed. During the primary core code execution, the auxiliary core code is reallocated from the flash memory to the RAM, and the auxiliary core is released from the reset. The hello\_world multicore application is now running

and a banner is displayed on the terminal. If this is not true, check your terminal settings and connections.

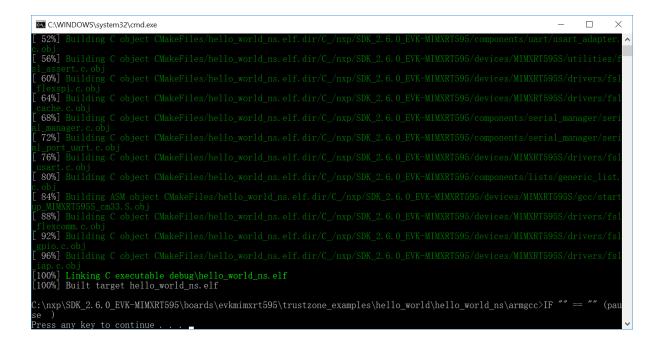


**Build a TrustZone example application** This section describes the steps to build and run a TrustZone application. The demo application build scripts are located in this folder:

```
 $$ < install\_dir > /boards / < board\_name > /trustzone\_examples / < application\_name > /[< core\_type >] / $$ < application\_name > _ns / armgcc $$ $$ < install\_dir > /boards / < board\_name > /trustzone\_examples / < application\_name > /[< core\_type >] / $$ < application\_name > _s / armgcc $$
```

Begin with a simple TrustZone version of the Hello World application. The TrustZone Hello World GCC build scripts are located in this folder:

Build both applications separately, following steps for single core examples as described in **Build** an example application. It is requested to build the application for the secure project first, because the non-secure project must know the secure project, since CMSE library is running the linker. It is not possible to finish the non-secure project linker with the secure project because the CMSE library is not ready.



**Run a TrustZone example application** When running a TrustZone application, the same prerequisites for J-Link/J-Link OpenSDA firmware, and the serial console as for the single core application, apply, as described in **Run an example application**.

To download and run the TrustZone application, perform steps 1 to 10, as described in **Run an example application**. These steps are common for both single core and TrustZone applications in Arm GCC.

# Then, run these commands:

- 1. arm-none-eabi-gdb.exe
- 2. target remote localhost:2331
- 3. monitor reset
- 4. monitor halt
- 5. monitor exec SetFlashDLNoRMWThreshold = 0x20000
- 7. load <install\_dir>/boards/evkmimxrt595/trustzone\_examples/hello\_world/hello\_world\_s/armgcc/debug/hello world s.elf
- 8. monitor reset

The application is now downloaded and halted. Execute the  ${\ensuremath{c}}$  command to start the demo application.

```
Command Prompt - arm-none-eabi-gdb
                                                                                                                                                                                                                                                                                                                                                                                                                                 C:\nxp\SDK_2.6.0_EVK-MIMXRT595\boards\evkmimxrt595\trustzone_examples\hello_world>arm-none-eabi-gdb
C:\Program Files (x86)\GNU Tools Arm Embedded\8 2018-q4-major\bin\arm-none-eabi-gdb.exe: warning: Couldn't determine a p
ath for the index cache directory.
GNU gdb (GNU Tools for Arm Embedded Processors 8-2018-q4-major) 8.2.50.20181213-git
Copyright (C) 2018 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later \http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.
Type "show copying" and "show warranty" for details.
This GDB was configured as "--host=i686-w64-mingw32 --target=arm-none-eabi".
Type "show configuration" for configuration details.
For bug reporting instructions, please see:
\http://www.gnu.org/software/gdb/bugs/>.
Find the GDB manual and other documentation resources online at:
\http://www.gnu.org/software/gdb/documentation/>.
                <http://www.gnu.org/software/gdb/documentation/</pre>
      or help, type "help
   or help, type help.
Type "apropos word" to search for commands related to "word".

(gdb) target remote localhost:2331

Remote debugging using localhost:2331

warning: No executable has been specified and target does not support determining executable automatically. Try using the "file" command.
 warning: No executable has been specified and target does determining executable automatically. Try using the "file 0x0001c04a in ?? () (gdb) load hello_world_ns/armgcc/debug/hello_world_ns.elf Loading section .interrupts, size 0x168 lma 0xc0000 Loading section .text, size 0x1630 lma 0xc180 Loading section .ARM, size 0x8 lma 0xc1eb0 Loading section .init_array, size 0x4 lma 0xc1eb8 Loading section .fini_array, size 0x4 lma 0xc1ebc Loading section .data, size 0x60 lma 0xc1ec0 Start address 0xc0234, load size 7944 Transfer rate: 74 KB/sec, 1324 bytes/write. (gdb) load hello_world_s/armgcc/debug/hello_world_s.elf Loading section .flash_config, size 0x200 lma 0x1007f400 Loading section .flash_config, size 0x200 lma 0x1007f400 Loading section .interrupts, size 0x168 lma 0x10080000 Loading section .ARM, size 0x8 lma 0x10084e44 Loading section .init_array, size 0x4 lma 0x10084ee0 Loading section .fini_array, size 0x4 lma 0x10084ee0 Loading section .gnu.sgstubs, size 0x20 lma 0x100bfe00 Start address 0x10080234, load size 20820 Transfer rate: 123 KB/sec, 2313 bytes/write.
    Transfer rate: 123 KB/sec, 2313 bytes/write.
      ontinuing.
      COM57 - PuTTY
   Hello from secure world!
   Entering normal world.
   Welcome in normal world!
    This is a text printed from normal world!
    Comparing two string as a callback to normal world
   String 1: Testl
   String 2: Test2
    Both strings are not equal!
```

# **MCUXpresso Config Tools**

MCUXpresso Config Tools can help configure the processor and generate initialization code for the on chip peripherals. The tools are able to modify any existing example project, or create a new configuration for the selected board or processor. The generated code is designed to be used with MCUXpresso SDK version 24.12.00 or later.

Following table describes the tools included in the MCUXpresso Config Tools.

Config Tool	Description	Im- age
Pins tool	For configuration of pin routing and pin electrical properties.	
Clock tool	For system clock configuration	(III)
Peripher- als tools	For configuration of other peripherals	P
TEE tool	Configures access policies for memory area and peripherals helping to protect and isolate sensitive parts of the application.	
Device Config- uration tool	Configures Device Configuration Data (DCD) contained in the program image that the Boot ROM code interprets to set up various on-chip peripherals prior to the program launch.	<u>*************************************</u>

MCUXpresso Config Tools can be accessed in the following products:

- **Integrated** in the MCUXpresso IDE. Config tools are integrated with both compiler and debugger which makes it the easiest way to begin the development.
- **Standalone version** available for download from www.nxp.com/mcuxpresso. Recommended for customers using IAR Embedded Workbench, Keil MDK μVision, or Arm GCC.
- **Online version** available on mcuxpresso.nxp.com. Recommended doing a quick evaluation of the processor or use the tool without installation.

Each version of the product contains a specific *Quick Start Guide* document MCUXpresso IDE Config Tools installation folder that can help start your work.

## **How to determine COM port**

This section describes the steps necessary to determine the debug COM port number of your NXP hardware development platform. All NXP boards ship with a factory programmed, onboard debug interface, whether it is based on MCU-Link or the legacy OpenSDA, LPC-Link2, P&E Micro OSJTAG interface. To determine what your specific board ships with, see *Default debug interfaces*.

1. **Linux**: The serial port can be determined by running the following command after the USB Serial is connected to the host:

```
$ dmesg | grep "ttyUSB"

[503175.307873] usb 3-12: cp210x converter now attached to ttyUSB0

[503175.309372] usb 3-12: cp210x converter now attached to ttyUSB1
```

There are two ports, one is for core0 debug console and the other is for core1.

2. **Windows**: To determine the COM port open Device Manager in the Windows operating system. Click the **Start** menu and type **Device Manager** in the search bar.

In the Device Manager, expand the **Ports (COM & LPT)** section to view the available ports. The COM port names are different for all the NXP boards.

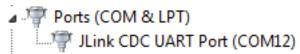
1. CMSIS-DAP/mbed/DAPLink interface:



### 2. P&E Micro:



# 3. **J-Link**:



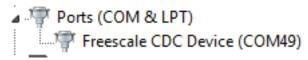
# 4. P&E Micro OSJTAG:

```
Ports (COM & LPT)

Ports (COM & LPT)

OSBDM/OSJTAG - CDC Serial Port (http://www.pemicro.com/osbdm, http://www.pemicro.com/opensda) (COM43)
```

## 5. MRB-KW01:



# **On-board Debugger**

This section describes the on-board debuggers used on NXP development boards.

On-board debugger MCU-Link MCU-Link is a powerful and cost effective debug probe that can be used seamlessly with MCUXpresso IDE, and is also compatible with 3rd party IDEs that support CMSIS-DAP protocol. MCU-Link also includes a USB to UART bridge feature (VCOM) that can be used to provide a serial connection between the target MCU and a host computer. MCU-Link features a high-speed USB interface for high performance debug. MCU-Link is compatible with Windows, MacOS and Linux. A free utility from NXP provides an easy way to install firmware updates.

On-board MCU-Link debugger supports CMSIS-DAP and J-Link firmware. See the table in *Default debug interfaces* to determine the default debug interface that comes loaded on your specific hardware platform.

# The corresponding host driver must be installed before debugging.

- For boards with CMSIS-DAP firmware, visit developer.mbed.org/handbook/Windows-serial-configuration and follow the instructions to install the Windows operating system serial driver. If running on Linux OS, this step is not required.
- If using J-Link with either a standalone debug pod or MCU-Link, install the J-Link software (drivers and utilities) from www.segger.com/jlink-software.html.

**Updating MCU-Link firmware** This firmware in this debug interface may be updated using the host computer utility called MCU-Link. This typically used when switching between the default debugger protocol (CMSIS-DAP) to SEGGER J-Link, or for updating this firmware with new releases of these. This section contains the steps to reprogram the debug probe firmware.

**Note:** If MCUXpresso IDE is used and the jumper making DFUlink is installed on the board (JP5 on some boards, but consult the board user manual or schematic for specific jumper number), MCU-Link debug probe boots to DFU mode, and MCUXpresso IDE automatically downloads the

CMSIS-DAP firmware to the probe before flash memory programming (after clicking **Debug**). Using DFU mode ensures that most up-to-date/compatible firmware is used with MCUXpresso IDE.

NXP provides the MCU-Link utility, which is the recommended tool for programming the latest versions of CMSIS-DAP and J-Link firmware onto MCU-Link or NXP boards. The utility can be downloaded from MCU-Link.

These steps show how to update the debugger firmware on your board for Windows operating system.

- 1. Install the MCU-Link utility.
- 2. Unplug the board's USB cable.
- 3. Make the DFU link (install the jumper labeled DFUlink).
- 4. Connect the probe to the host via USB (use Link USB connector).
- 5. Open a command shell and call the appropriate script located in the MCU-Link installation directory (<MCU-Link install dir>).
  - 1. To program CMSIS-DAP debug firmware: <MCU-Link install dir>/scripts/program\_CMSIS
  - 2. To program J-Link debug firmware: <MCU-Link install dir>/scripts/program\_JLINK
- 6. Remove DFU link (remove the jumper installed in Step 3).
- 7. Repower the board by removing the USB cable and plugging it in again.

**On-board debugger LPC-Link** LPC-Link 2 is an extensible debug probe that can be used seamlessly with MCUXpresso IDE, and is also compatible with 3rd party IDEs that support CMSIS-DAP protocol. MCU-Link also includes a USB to UART bridge feature (VCOM) that can be used to provide a serial connection between the target MCU and a host computer. LPC-Link 2 is compatible with Windows, MacOS and Linux. A free utility from NXP provides an easy way to install firmware updates.

On-board LPC-Link 2 debugger supports CMSIS-DAP and J-Link firmware. See the table in *Default debug interfaces* to determine the default debug interface that comes loaded on your specific hardware platform.

## The corresponding host driver must be installed before debugging.

- For boards with CMSIS-DAP firmware, visit developer.mbed.org/handbook/Windowsserial-configuration and follow the instructions to install the Windows operating system serial driver. If running on Linux OS, this step is not required.
- If using J-Link with either a standalone debug pod or MCU-Link, install the J-Link software (drivers and utilities) from www.segger.com/jlink-software.html.

**Updating LPC-Link firmware** The LPCXpresso hardware platform comes with a CMSIS-DAP-compatible debug interface (known as LPC-Link2). This firmware in this debug interface may be updated using the host computer utility called LPCScrypt. This typically used when switching between the default debugger protocol (CMSIS-DAP) to SEGGER J-Link, or for updating this firmware with new releases of these. This section contains the steps to reprogram the debug probe firmware.

**Note:** If MCUXpresso IDE is used and the jumper making DFUlink is installed on the board (JP5 on some boards, but consult the board user manual or schematic for specific jumper number), LPC-Link2 debug probe boots to DFU mode, and MCUXpresso IDE automatically downloads the CMSIS-DAP firmware to the probe before flash memory programming (after clicking **Debug**). Using DFU mode ensures that most up-to-date/compatible firmware is used with MCUXpresso IDE.

NXP provides the LPCScrypt utility, which is the recommended tool for programming the latest versions of CMSIS-DAP and J-Link firmware onto LPC-Link2 or LPCXpresso boards. The utility can be downloaded from LPCScrypt.

These steps show how to update the debugger firmware on your board for Windows operating system. For Linux OS, follow the instructions described in LPCScrypt user guide (LPCScrypt, select **LPCScrypt**, and then the documentation tab).

- 1. Install the LPCScript utility.
- 2. Unplug the board's USB cable.
- 3. Make the DFU link (install the jumper labeled DFUlink).
- 4. Connect the probe to the host via USB (use Link USB connector).
- 5. Open a command shell and call the appropriate script located in the LPCScrypt installation directory (<LPCScrypt install dir>).
  - 1. To program CMSIS-DAP debug firmware: <LPCScrypt install dir>/scripts/program\_CMSIS
  - 2. To program J-Link debug firmware: <LPCScrypt install dir>/scripts/program\_JLINK
- 6. Remove DFU link (remove the jumper installed in Step 3).
- 7. Repower the board by removing the USB cable and plugging it in again.

**On-board debugger OpenSDA** OpenSDA/OpenSDAv2 is a serial and debug adapter that is built into several NXP evaluation boards. It provides a bridge between your computer (or other USB host) and the embedded target processor, which can be used for debugging, flash programming, and serial communication, all over a simple USB cable.

The difference is the firmware implementation: OpenSDA: Programmed with the proprietary P&E Micro developed bootloader. P&E Micro is the default debug interface app. OpenSDAv2: Programmed with the open-sourced CMSIS-DAP/mbed bootloader. CMSIS-DAP is the default debug interface app.

See the table in *Default debug interfaces* to determine the default debug interface that comes loaded on your specific hardware platform.

# The corresponding host driver must be installed before debugging.

- For boards with CMSIS-DAP firmware, visit developer.mbed.org/handbook/Windows-serial-configuration and follow the instructions to install the Windows operating system serial driver. If running on Linux OS, this step is not required.
- For boards with a P&E Micro interface, see PE micro to download and install the P&E Micro Hardware Interface Drivers package.

**Updating OpenSDA firmware** Any NXP hardware platform that comes with an OpenSDA-compatible debug interface has the ability to update the OpenSDA firmware. This typically means to switch from the default application (either CMSIS-DAP or P&E Micro) to a SEGGER J-Link. This section contains the steps to switch the OpenSDA firmware to a J-Link interface. However, the steps can be applied to restoring the original image also. For reference, OpenSDA firmware files can be found at the links below:

- J-Link: Download appropriate image from www.segger.com/opensda.html. Choose the appropriate J-Link binary based on the table in *Default debug interfaces*. Any OpenSDA v1.0 interface should use the standard OpenSDA download (in other words, the one with no version). For OpenSDA 2.0 or 2.1, select the corresponding binary.
- CMSIS-DAP: CMSIS-DAP OpenSDA firmware is available at www.nxp.com/opensda.

• P&E Micro: Downloading P&E Micro OpenSDA firmware images requires registration with P&E Micro (www.pemicro.com).

Perform the following steps to update the OpenSDA firmware on your board for Windows and Linux OS users:

- 1. Unplug the board's USB cable.
- 2. Press the **Reset** button on the board. While still holding the button, plug the USB cable back into the board.
- 3. When the board re-enumerates, it shows up as a disk drive called **MAINTENANCE**.



4. Drag and drop the new firmware image onto the MAINTENANCE drive.

**Note:** If for any reason the firmware update fails, the board can always reenter maintenance mode by holding down **Reset** button and power cycling.

These steps show how to update the OpenSDA firmware on your board for Mac OS users.

- 1. Unplug the board's USB cable.
- 2. Press the **Reset** button of the board. While still holding the button, plug the USB cable back into the board.
- 3. For boards with OpenSDA v2.0 or v2.1, it shows up as a disk drive called **BOOTLOADER** in **Finder**. Boards with OpenSDA v1.0 may or may not show up depending on the bootloader version. If you see the drive in **Finder**, proceed to the next step. If you do not see the drive in Finder, use a PC with Windows OS 7 or an earlier version to either update the OpenSDA firmware, or update the OpenSDA bootloader to version 1.11 or later. The bootloader update instructions and image can be obtained from P&E Microcomputer website.
- 4. For OpenSDA v2.1 and OpenSDA v1.0 (with bootloader 1.11 or later) users, drag the new firmware image onto the BOOTLOADER drive in **Finder**.
- 5. For OpenSDA v2.0 users, type these commands in a Terminal window:

```
> sudo mount -u -w -o sync /Volumes/BOOTLOADER
> cp -X <path to update file> /Volumes/BOOTLOADER
```

**Note:** If for any reason the firmware update fails, the board can always reenter bootloader mode by holding down the **Reset** button and power cycling.

**On-board debugger Multilink** An on-board Multilink debug circuit provides a JTAG interface and a power supply input through a single micro-USB connector. It is a hardware interface that allows PC software to debug and program a target processor through its debug port.

# The host driver must be installed before debugging.

• See PE micro to download and install the P&E Micro Hardware Interface Drivers package.

**On-board debugger OSJTAG** An on-board OSJTAG debug circuit provides a JTAG interface and a power supply input through a single micro-USB connector. It is a hardware interface that allows PC software to debug and program a target processor through its debug port.

# The host driver must be installed before debugging.

• See PE micro to download and install the P&E Micro Hardware Interface Drivers package.

# **Default debug interfaces**

The MCUXpresso SDK supports various hardware platforms that come loaded with various factory programmed debug interface configurations. The following table lists the hardware platforms supported by the MCUXpresso SDK, their default debug firmware, and any version information that helps differentiate a specific interface configuration.

continues on next page

Table 1 – continued from previous page
--

Hardware platform	Default debugger firmware	On-board debugger probe
•	CMSIS-DAP	LPC-Link2
LPCXpresso54S018 LPCXpresso54S018M	CMSIS-DAP	LPC-Link2
LPCXpresso55S06	CMSIS-DAP	LPC-Link2
	CMSIS-DAP	LPC-Link2
LPCXpresso55S16		
LPCXpresso55S28	CMSIS-DAP	LPC-Link2
LPCXpresso55S36	CMSIS-DAP	MCU-Link
LPCXpresso55S69	CMSIS-DAP	LPC-Link2
LPCXpresso802	CMSIS-DAP	LPC-Link2
LPCXpresso804	CMSIS-DAP	LPC-Link2
LPCXpresso824MAX	CMSIS-DAP	LPC-Link2
LPCXpresso845MAX	CMSIS-DAP	LPC-Link2
LPCXpresso860MAX	CMSIS-DAP	LPC-Link2
MC56F80000-EVK	P&E Micro	Multilink
MC56F81000-EVK	P&E Micro	Multilink
MC56F83000-EVK	P&E Micro	OSJTAG
MCIMX93-EVK	N/A	N/A
MCIMX93-QSB	N/A	N/A
MCIMX93AUTO-EVK	N/A	N/A
MCX-N5XX-EVK	CMSIS-DAP	MCU-Link
MCX-N9XX-EVK	CMSIS-DAP	MCU-Link
MCX-W71-EVK	CMSIS-DAP	MCU-Link
MCX-W72-EVK	CMSIS-DAP	MCU-Link
MIMXRT1024-EVK	CMSIS-DAP	LPC-Link2
MIMXRT1040-EVK	CMSIS-DAP	LPC-Link2
MIMXRT1060-EVKB	CMSIS-DAP	LPC-Link2
MIMXRT1060-EVKC	CMSIS-DAP	MCU-Link
MIMXRT1160-EVK	CMSIS-DAP	LPC-Link2
MIMXRT1170-EVKB	CMSIS-DAP	MCU-Link
MIMXRT1180-EVK	CMSIS-DAP	MCU-Link
MIMXRT685-AUD-EVK	CMSIS-DAP	LPC-Link2
MIMXRT700-EVK	CMSIS-DAP	MCU-Link
RD-RW612-BGA	CMSIS-DAP	MCU-Link
TWR-KM34Z50MV3	P&E Micro	OpenSDA v1
TWR-KM34Z75M	P&E Micro	OpenSDA v1
TWR-KM35Z75M	CMSIS-DAP	OpenSDA v2
TWR-MC56F8200	P&E Micro	OSJTAG
TWR-MC56F8400	P&E Micro	OSJTAG

# How to define IRQ handler in CPP files

With MCUXpresso SDK, users could define their own IRQ handler in application level to override the default IRQ handler. For example, to override the default PIT\_IRQHandler define in startup\_DEVICE.s, application code like app.c can be implement like:

```
// c
void PIT_IRQHandler(void)
{
    // Your code
}
```

When application file is CPP file, like app.cpp, then  $\operatorname{extern}$  "C" should be used to ensure the function prototype alignment.

```
// cpp
extern "C" {
   void PIT_IRQHandler(void);
}
void PIT_IRQHandler(void)
{
   // Your code
}
```

# 1.3 Getting Started with MCUXpresso SDK GitHub

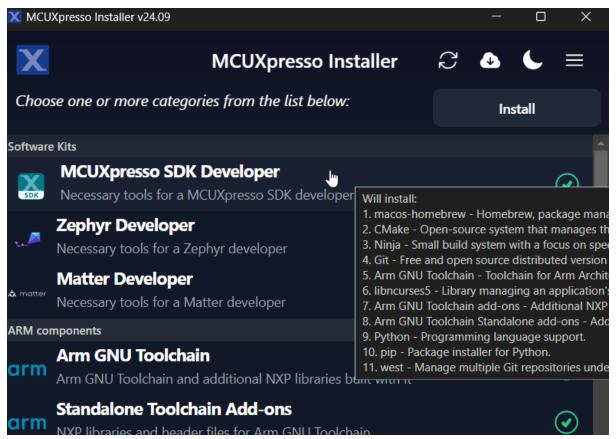
# 1.3.1 Getting Started with MCUXpresso SDK Repository

### **Installation**

### **NOTE**

If the installation instruction asks/selects whether to have the tool installation path added to the PATH variable, agree/select the choice. This option ensures that the tool can be used in any terminal in any path. *Verify the installation* after each tool installation.

**Install Prerequisites with MCUXpresso Installer** The MCUXpresso Installer offers a quick and easy way to install the basic tools needed. The MCUXpresso Installer can be obtained from https://github.com/nxp-mcuxpresso/vscode-for-mcux/wiki/Dependency-Installation. The MCUXpresso Installer is an automated installation process, simply select MCUXpresso SDK Developer from the menu and click install. If you prefer to install the basic tools manually, refer to the next section.



### Alternative: Manual Installation

### **Basic tools**

Git is a free and open source distributed version control system. Git is designed to handle everything from small to large projects with speed and efficiency. To install Git, visit the official Git website. Download the appropriate version(you may use the latest one) for your operating system (Windows, macOS, Linux). Then run the installer and follow the installation instructions.

User git --version to check the version if you have a version installed.

Then configure your username and email using the commands:

```
git config --global user.name "Your Name"
git config --global user.email "youremail@example.com"
```

**Python** Install python 3.10 or latest. Follow the Python Download guide.

Use python --version to check the version if you have a version installed.

# **West** Please use the west version equal or greater than 1.2.0

```
# Note: you can add option '--default-timeout=1000' if you meet connection issue. Or you may set a different_u source using option '-i'.

# for example, in China you could try: pip install -U west -i https://pypi.tuna.tsinghua.edu.cn/simple pip install -U west
```

# **Build And Configuration System**

**CMake** It is strongly recommended to use CMake version equal or later than 3.30.0. You can get latest CMake distributions from the official CMake download page.

For Windows, you can directly use the .msi installer like cmake-3.31.4-windows-x86\_64.msi to install.

For Linux, CMake can be installed using the system package manager or by getting binaries from the official CMake download page.

After installation, you can use cmake --version to check the version.

**Ninja** Please use the ninja version equal or later than 1.12.1.

By default, Windows comes with the Ninja program. If the default Ninja version is too old, you can directly download the ninja binary and register the ninja executor location path into your system path variable to work.

For Linux, you can use your system package manager or you can directly download the ninja binary to work.

After installation, you can use ninja --version to check the version.

**Kconfig** MCUXpresso SDK uses Kconfig python implementation. We customize it based on our needs and integrate it into our build and configuration system. The Kconfiglib sources are placed under mcuxsdk/scripts/kconfig folder.

Please make sure python environment is setup ready then you can use the Kconfig.

**Ruby** Our build system supports IDE project generation for iar, mdk, codewarrior and xtensa to provide OOBE from build to debug. This feature is implemented with ruby. You can follow the guide ruby environment setup to setup the ruby environment. Since we provide a built-in portable ruby, it is just a simple one cmd installation.

If you only work with CLI, you can skip this step.

**Toolchain** MCUXpresso SDK supports all mainstream toolchains for embedded development. You can install your used or interested toolchains following the guides.

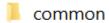
Toolchain	Download and Installation Guide	Note		
Armgcc	Arm GNU Toolchain Install Guide	ARMGCC toolchain	is	default
IAR	IAR Installation and Licensing quick reference guide			
MDK	MDK Installation			
Armclang	Installing Arm Compiler for Embedded			
Zephyr	Zephyr SDK			
Codewarrior	NXP CodeWarrior			
Xtensa	Tensilica Tools			
NXP S32Compiler RISC- V Zen-V	NXP Website			

After you have installed the toolchains, register them in the system environment variables. This will allow the west build to recognize them:

Toolchain	Environ- ment Variable	Example	Cmd Line Ar- gument
Armgcc	AR- MGCC_DIR	C:\armgcc for windows/usr for Linux. Typically arm-none-eabi-* is installed under /usr/bin	– toolchain armgcc
IAR	IAR_DIR	C:\iar\ewarm-9.60.3 for Windows/opt/iarsystems/bxarm-9.60.3 for Linux	toolchain
MDK	MDK_DIR	$C:\koliver \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	– toolchain mdk
Armclang	ARM- CLANG_DIF	C:\ArmCompilerforEmbedded6.22 for Windows/opt/ ArmCompilerforEmbedded6.21 for Linux	– toolchain mdk
Zephyr	ZEPHYR_SL	c:\NXP\zephyr-sdk- <version> for windows/opt/zephyr-sdk-<version> for Linux</version></version>	– toolchain zephyr
CodeWar- rior	CW_DIR	$\mbox{C:}\ensuremath{\operatorname{Freescale}}\ensuremath{\operatorname{CW}}\ensuremath{\operatorname{MCU}}\ensuremath{\operatorname{v11.2}}\xspace$ for windowsCodeWarrior is not supported with Linux	toolchain code- warrior
Xtensa	XCC_DIR	$\label{lem:cosx} C: \textbf{C:} \textbf{XtDevTools} \\ \textbf{Install} \\ \textbf{Tools} \\ \textbf{for} \\ \textbf{windows/opt/xtensa/XtDevTools/install/tools/RI-2023.11-Linux/XtensaTools} \\ \textbf{for} \\ \textbf{Linux} \\ \textbf{XtensaTools} \\ X$	– toolchain xtensa
NXP S32Compiler RISC-V Zen-V	RISCVL- LVM_DIR	$\label{lem:condition} C:\riscv-llvm-win32\_b298\_b298\_2024.08.12  \mbox{for Windows/opt/riscv-llvm-Linux-x64\_b298\_b298\_2024.08.12} \\ \mbox{for Linux}$	– toolchain riscvl- lvm

• The <toolchain>\_DIR is the root installation folder, not the binary location folder. For IAR, it is directory containing following installation folders:







- MDK IDE using armclang toolchain only officially supports Windows. In Linux, please directly use armclang toolchain by setting ARMCLANG\_DIR. In Windows, since most Keil users will install MDK IDE instead of standalone armclang toolchain, the MDK\_DIR has higher priority than ARMCLANG\_DIR.
- For Xtensa toolchain, please set the XTENSA\_CORE environment variable. Here's an example list:

Device Core	XTENSA_CORE
RT500 fusion1	$nxp_rt500_RI23_11_newlib$
RT600 hifi4	$nxp_rt600_RI23_11_newlib$
RT700 hifi1	$rt700_hifi1_RI23_11_nlib$
RT700 hifi4	t700_hifi4_RI23_11_nlib
i.MX8ULP fusion1	$fusion\_nxp02\_dsp\_prod$

• In Windows, the short path is used in environment variables. If any toolchain is using the long path, you can open a command window from the toolchain folder and use below command to get the short path: for %i in (.) do echo %~fsi

**Tool installation check** Once installed, open a terminal or command prompt and type the associated command to verify the installation.

If you see the version number, you have successfully installed the tool. Else, check whether the tool's installation path is added into the PATH variable. You can add the installation path to the PATH with the commands below:

• Windows: Open command prompt or powershell, run below command to show the user PATH variable.

```
reg query HKEY_CURRENT_USER\Environment /v PATH
```

The tool installation path should be C:\Users\xxx\AppData\Local\Programs\Git\cmd. If the path is not seen in the output from above, append the path value to the PATH variable with the command below:

```
reg add HKEY_CURRENT_USER\Environment /v PATH /d "%PATH%;C:\Users\xxx\AppData\ \Local\Programs\Git\cmd"
```

Then close the command prompt or powershell and verify the tool command again.

- Linux:
  - 1. Open the \$HOME/.bashrc file using a text editor, such as vim.
  - 2. Go to the end of the file.
  - 3. Add the line which appends the tool installation path to the PATH variable and export PATH at the end of the file. For example, export PATH="/Directory1:\$PATH".
  - 4. Save and exit.
  - 5. Execute the script with source .bashrc or reboot the system to make the changes live. To verify the changes, run echo \$PATH.
- · macOS:
  - 1. Open the \$HOME/.bash\_profile file using a text editor, such as nano.
  - 2. Go to the end of the file.
  - 3. Add the line which appends the tool installation path to the PATH variable and export PATH at the end of the file. For example, export PATH="/Directory1:\$PATH".
  - 4. Save and exit.
  - 5. Execute the script with source .bash\_profile or reboot the system to make the changes live. To verify the changes, run echo \$PATH.

## Get MCUXpresso SDK Repo

**Establish SDK Workspace** To get the MCUXpresso SDK repository, use the west tool to clone the manifest repository and checkout all the west projects.

```
# Initialize west with the manifest repository
west init -m https://github.com/nxp-mcuxpresso/mcuxsdk-manifests/ mcuxpresso-sdk

# Update the west projects
cd mcuxpresso-sdk
west update

# Allow the usage of west extensions provided by MCUXpresso SDK
west config commands.allow_extensions true
```

**Install Python Dependency(If do tool installation manually)** To create a Python virtual environment in the west workspace core repo directory mcuxsdk, follow these steps:

1. Navigate to the core directory:

```
cd mcuxsdk
```

2. [Optional] Create and activate the virtual environment: If you don't want to use the python virtual environment, skip this step. We strongly suggest you use venv to avoid conflicts with other projects using python.

```
python -m venv .venv

# For Linux/MacOS
source .venv/bin/activate

# For Windows
.\.venv\Scripts\activate

# If you are using powershell and see the issue that the activate script cannot be run.

# You may fix the issue by opening the powershell as administrator and run below command:
powershell Set-ExecutionPolicy RemoteSigned

# then run above activate command again.
```

Once activated, your shell will be prefixed with (.venv). The virtual environment can be deactivated at any time by running deactivate command.

Remember to activate the virtual environment every time you start working in this directory. If you are using some modern shell like zsh, there are some powerful plugins to help you auto switch venv among workspaces. For example, zsh-autoswitch-virtualenv.

3. Install the required Python packages:

```
# Note: you can add option '--default-timeout=1000' if you meet connection issue. Or you may set audifferent source using option '-i'.
# for example, in China you could try: pip3 install -r mcuxsdk/scripts/requirements.txt -i https://pypi.utuna.tsinghua.edu.cn/simple pip install -r scripts/requirements.txt
```

# **Explore Contents**

This section helps you build basic understanding of current fundamental project content and guides you how to build and run the provided example project in whole SDK delivery.

**Folder View** The whole MCUXpresso SDK project, after you have done the west init and west update operations follow the guideline at *Getting Started Guide*, have below folder structure:

Folder	Description
mani- fests mcuxsdk	Manifest repo, contains the manifest file to initialize and update the west workspace.  The MCUXpresso SDK source code, examples, middleware integration and script files.

All the projects record in the Manifest repo are checked out to the folder mcuxsdk/, the layout of mcuxsdk folder is shown as below:

Folder	Description
arch	Arch related files such as ARM CMSIS core files, RISC-V files and the build files related to the architecture.
cmake	The cmake modules, files which organize the build system.
com- po- nents	Software components.
de- vices	Device support package which categorized by device series. For each device, header file, feature file, startup file and linker files are provided, also device specific drivers are included.
docs	Documentation source and build configuration for this sphinx built online documentation.
drivers	Peripheral drivers.
ex- am- ples	Various demos and examples, support files on different supported boards. For each board support, there are board configuration files.
mid- dle- ware	Middleware components integrated into SDK.
rtos	Rtos components integrated into SDK.
scripts	Script files for the west extension command and build system support.
svd	Svd files for devices, this is optional because of large size. Customers run west manifest config group.filter +optional and west update mcux-soc-svd to get this folder.

**Examples Project** The examples project is part of the whole SDK delivery, and locates in the folder mcuxsdk/examples of west workspace.

Examples files are placed in folder of <example\_category>, these examples include (but are not limited to)

- demo\_apps: Basic demo set to start using SDK, including hello\_world and led\_blinky.
- driver\_examples: Simple applications that show how to use the peripheral drivers for a single use case. These applications typically only use a single peripheral but there are cases where multiple peripherals are used (for example, SPI transfer using DMA).

Board porting layers are placed in folder of  $\_boards/< board\_name>$  which aims at providing the board specific parts for examples code mentioned above.

## Run a demo using MCUXpresso for VS Code

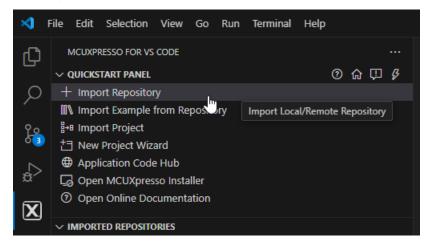
This section explains how to configure MCUXpresso for VS Code to build, run, and debug example applications. This guide uses the hello\_world demo application as an example. However, these

steps can be applied to any example application in the MCUXpresso SDK.

**Build an example application** This section assumes that the user has already obtained the SDK as outlined in *Get MCUXpresso SDK Repo*.

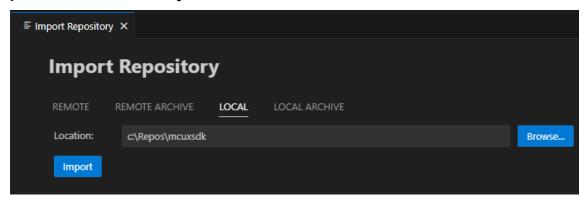
To build an example application:

1. Import the SDK into your workspace. Click **Import Repository** from the **QUICKSTART PANEL**.



**Note:** You can import the SDK in several ways. Refer to MCUXpresso for VS Code Wiki for details.

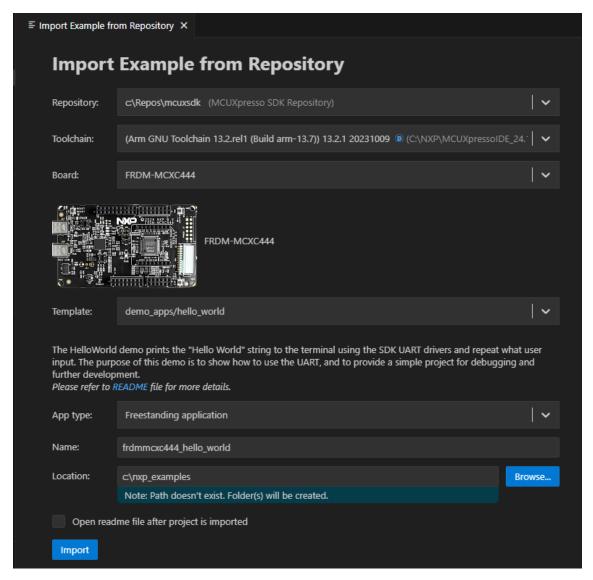
Select **Local** if you've already obtained the SDK as seen in *Get MCUXpresso SDK Repo*. Select your location and click **Import**.



2. Click Import Example from Repository from the QUICKSTART PANEL.

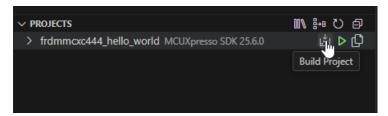


In the dropdown menu, select the MCUXpresso SDK, the Arm GNU Toolchain, your board, template, and application type. Click **Import**.



**Note:** The MCUXpresso SDK projects can be imported as **Repository applications** or **Freestanding applications**. The difference between the two is the import location. Projects imported as Repository examples will be located inside the MCUXpresso SDK, whereas Freestanding examples can be imported to a user-defined location. Select between these by designating your selection in the **App type** dropdown menu.

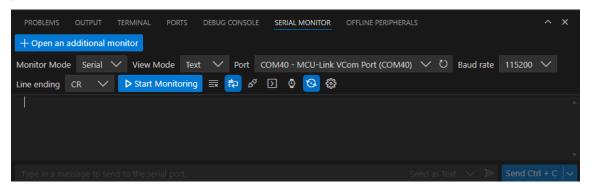
- 3. VS Code will prompt you to confirm if the imported files are trusted. Click Yes.
- 4. Navigate to the **PROJECTS** view. Find your project and click the **Build Project** icon.



The integrated terminal will open at the bottom and will display the build output.

**Run an example application Note:** for full details on MCUXpresso for VS Code debug probe support, see MCUXpresso for VS Code Wiki.

1. Open the **Serial Monitor** from the VS Code's integrated terminal. Select the VCom Port for your device and set the baud rate to 115200.

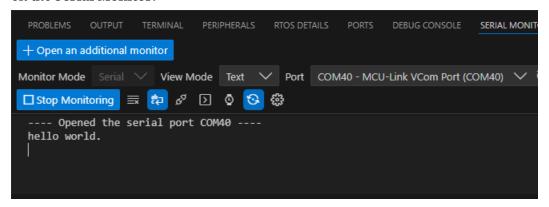


2. Navigate to the **PROJECTS** view and click the play button to initiate a debug session.



The debug session will begin. The debug controls are initially at the top.

3. Click **Continue** on the debug controls to resume execution of the code. Observe the output on the **Serial Monitor**.



# Running a demo using ARMGCC CLI/IAR/MDK

**Supported Boards** Use the west extension west list\_project to understand the board support scope for a specified example. All supported build command will be listed in output:

(continued from previous page)

The supported toolchains and build targets for an example are decided by the example-self example.yml and board example.yml, please refer Example Toolchains and Targets for more details.

**Build the project** Use west build -h to see help information for west build command. Compared to zephyr's west build, MCUXpresso SDK's west build command provides following additional options for mcux examples:

- --toolchain: specify the toolchain for this build, default armgcc.
- --config: value for CMAKE\_BUILD\_TYPE. If not provided, build system will get all the example supported build targets and use the first debug target as the default one. Please refer Example Toolchains and Targets for more details about example supported build targets.

Here are some typical usages for generating a SDK example:

```
# Generate example with default settings, default used device is the mainset MK22F51212
west build -b frdmk22f examples/demo_apps/hello_world

# Just print cmake commands, do not execute it
west build -b frdmk22f examples/demo_apps/hello_world --dry-run

# Generate example with other toolchain like iar, default armgcc
west build -b frdmk22f examples/demo_apps/hello_world --toolchain iar

# Generate example with other config type
west build -b frdmk22f examples/demo_apps/hello_world --config release

# Generate example with other devices with --device
west build -b frdmk22f examples/demo_apps/hello_world --device MK22F12810 --config release
```

For multicore devices, you shall specify the corresponding core id by passing the command line argument -Dcore\_id. For example

```
west build -b evkbmimxrt1170 examples/demo_apps/hello_world --toolchain iar -Dcore_id=cm7 --config_ \rightarrowflexspi_nor_debug
```

For shield, please use the --shield to specify the shield to run, like

```
west build -b mimxrt700evk --shield a8974 examples/issdk_examples/sensors/fxls8974cf/fxls8974cf_poll - \rightarrow Dcore_id=cm33_core0
```

**Sysbuild(System build)** To support multicore project building, we ported Sysbuild from Zephyr. It supports combine multiple projects for compilation. You can build all projects by adding --sysbuild for main application. For example:

```
west build -b evkbmimxrt1170 --sysbuild ./examples/multicore_examples/hello_world/primary -Dcore_ \rightarrowid=cm7 --config flexspi_nor_debug --toolchain=armgcc -p always
```

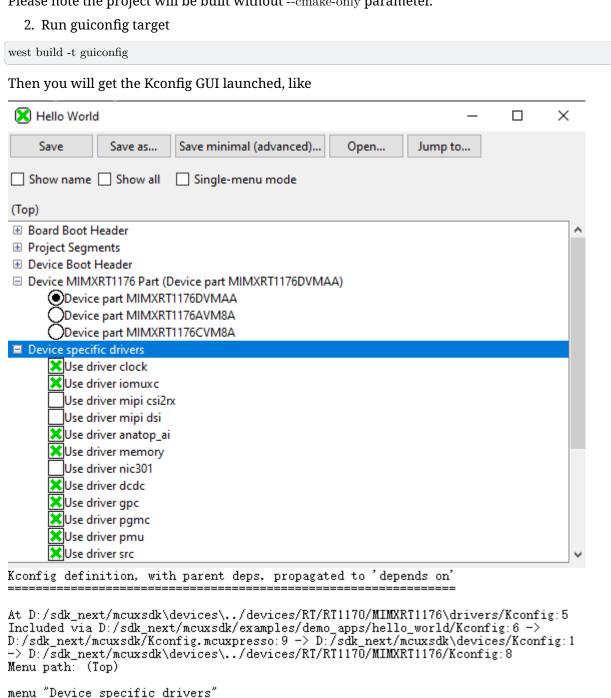
For more details, please refer to System build.

**Config a Project** Example in MCUXpresso SDK is configured and tested with pre-defined configuration. You can follow steps blow to change the configuration.

1. Run cmake configuration

 $\begin{tabular}{ll} west build -b evkbmimxrt1170 examples/demo\_apps/hello\_world -Dcore\_id=cm7 --cmake-only -p \\ \end{tabular}$ 

Please note the project will be built without --cmake-only parameter.



You can reconfigure the project by selecting/deselecting Kconfig options.

After saving and closing the Kconfig GUI, you can directly run west build to build with the new configuration.

**Flash** *Note*: Please refer Flash and Debug The Example to enable west flash/debug support. Flash the hello\_world example:

```
west flash -r linkserver
```

**Debug** Start a gdb interface by following command:

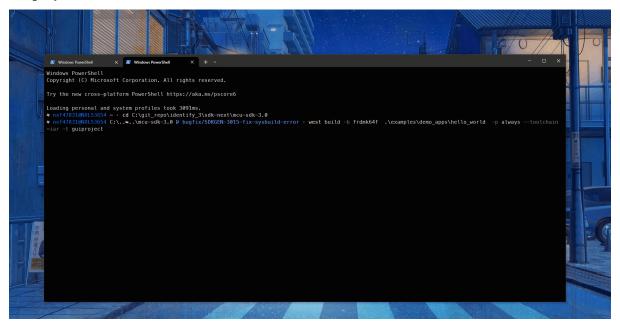
```
west debug -r linkserver
```

**Work with IDE Project** The above build functionalities are all with CLI. If you want to use the toolchain IDE to work to enjoy the better user experience especially for debugging or you are already used to develop with IDEs like IAR, MDK, Xtensa and CodeWarrior in the embedded world, you can play with our IDE project generation functionality.

This is the cmd to generate the evkbmimxrt1170 hello\_world IAR IDE project files.

```
west build -b evkbmimxrt1170 examples/demo_apps/hello_world --toolchain iar -Dcore_id=cm7 --configusflexspi_nor_debug -p always -t guiproject
```

By default, the IDE project files are generated in mcuxsdk/build/<toolchain> folder, you can open the project file with the IDE tool to work:



Note, please follow the *Installation* to setup the environment especially make sure that *ruby* has been installed.

# 1.4 Release Notes

# 1.4.1 MCUXpresso SDK Release Notes

### **Overview**

The MCUXpresso SDK is a comprehensive software enablement package designed to simplify and accelerate application development with Arm Cortex-M-based devices from NXP, including its general purpose, crossover and Bluetooth-enabled MCUs. MCUXpresso SW and Tools for DSC

further extends the SDK support to current 32-bit Digital Signal Controllers. The MCUXpresso SDK includes production-grade software with integrated RTOS (optional), integrated enabling software technologies (stacks and middleware), reference software, and more.

In addition to working seamlessly with the MCUXpresso IDE, the MCUXpresso SDK also supports and provides example projects for various toolchains. The Development tools chapter in the associated Release Notes provides details about toolchain support for your board. Support for the MCUXpresso Config Tools allows easy cloning of existing SDK examples and demos, allowing users to leverage the existing software examples provided by the SDK for their own projects.

Underscoring our commitment to high quality, the MCUXpresso SDK is MISRA compliant and checked with Coverity static analysis tools. For details on MCUXpresso SDK, see MCUXpresso-SDK: Software Development Kit for MCUXpresso.

# **MCUXpresso SDK**

As part of the MCUXpresso software and tools, MCUXpresso SDK is the evolution of Kinetis SDK, includes support for LPC, DSC,PN76, and i.MX System-on-Chip (SoC). The same drivers, APIs, and middleware are still available with support for Kinetis, LPC, DSC, and i.MX silicon. The MCUX-presso SDK adds support for the MCUXpresso IDE, an Eclipse-based toolchain that works with all MCUXpresso SDKs. Easily import your SDK into the new toolchain to access to all of the available components, examples, and demos for your target silicon. In addition to the MCUXpresso IDE, support for the MCUXpresso Config Tools allows easy cloning of existing SDK examples and demos, allowing users to leverage the existing software examples provided by the SDK for their own projects.

In order to maintain compatibility with legacy Freescale code, the filenames and source code in MCUXpresso SDK containing the legacy Freescale prefix FSL has been left as is. The FSL prefix has been redefined as the NXP Foundation Software Library.

#### **Development tools**

The MCUXpresso SDK was tested with following development tools. Same versions or above are recommended.

- MCUXpresso IDE, Rev. 25.06.xx
- IAR Embedded Workbench for Arm, version is 9.60.4
- Keil MDK, version is 5.41
- MCUXpresso for VS Code v25.06
- GCC Arm Embedded Toolchain 14.2.x

# Supported development systems

This release supports board and devices listed in following table. The board and devices in bold were tested in this release.

Development boards	MCU devices		
LPCXpresso802	LPC802M001JDH16, LPC802M011JDH20, LPC8	<b>LPC802M001JDH20</b> , 802UK	LPC802M001JHI33,

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#### MCUXpresso SDK release package

The MCUXpresso SDK release package content is aligned with the silicon subfamily it supports. This includes the boards, CMSIS, devices, middleware, and RTOS support.

**Device support** The device folder contains the whole software enablement available for the specific System-on-Chip (SoC) subfamily. This folder includes clock-specific implementation, device register header files, device register feature header files, and the system configuration source files. Included with the standard SoC support are folders containing peripheral drivers, toolchain support, and a standard debug console. The device-specific header files provide a direct access to the microcontroller peripheral registers. The device header file provides an overall SoC memory mapped register definition. The folder also includes the feature header file for each peripheral on the microcontroller. The toolchain folder contains the startup code and linker files for each supported toolchain. The startup code efficiently transfers the code execution to the main() function.

**Board support** The boards folder provides the board-specific demo applications, driver examples, and middleware examples.

**Demo application and other examples** The demo applications demonstrate the usage of the peripheral drivers to achieve a system level solution. Each demo application contains a readme file that describes the operation of the demo and required setup steps. The driver examples demonstrate the capabilities of the peripheral drivers. Each example implements a common use case to help demonstrate the driver functionality.

#### **Middleware**

**CMSIS DSP Library** The MCUXpresso SDK is shipped with the standard CMSIS development pack, including the prebuilt libraries.

**FreeMASTER** FreeMASTER communication driver for 32-bit platforms.

#### **Release contents**

Provides an overview of the MCUXpresso SDK release package contents and locations.

Deliverable	Location	
Boards	INSTALL_DIR/boards	
Demo Applications	INSTALL_DIR/boards/ <board_name>/demo_apps</board_name>	
Driver Examples	INSTALL_DIR/boards/ <board_name>/driver_example</board_name>	
eIQ examples	INSTALL_DIR/boards/ <board_name>/eiq_examples</board_name>	
Board Project Template for MCUXpresso IDE NPW	INSTALL_DIR/boards/ <board_name>/project_temp</board_name>	
Driver, SoC header files, extension header files and	INSTALL_DIR/devices/ <device_name></device_name>	
feature header files, utilities		
CMSIS drivers	INSTALL_DIR/devices/ <device_name>/cmsis_drive</device_name>	
Peripheral drivers	INSTALL_DIR/devices/ <device_name>/drivers</device_name>	
Toolchain linker files and startup code	INSTALL_DIR/devices/ <device_name>/<toolchain_n< td=""></toolchain_n<></device_name>	
Utilities such as debug console	INSTALL_DIR/devices/ <device_name>/utilities</device_name>	
Device Project Template for MCUXpresso IDE NPW	INSTALL_DIR/devices/ <device_name>/project_tem</device_name>	
CMSIS Arm Cortex-M header files, DSP library source	INSTALL_DIR/CMSIS	
Components and board device drivers	INSTALL_DIR/components	
RTOS	INSTALL_DIR/rtos	
Release Notes, Getting Started Document and other	INSTALL_DIR/docs	
documents		
Tools such as shared cmake files	INSTALL_DIR/tools	
Middleware	INSTALL_DIR/middleware	

# **Known issues**

This section lists the known issues, limitations, and/or workarounds.

# Cannot add SDK components into FreeRTOS projects

It is not possible to add any SDK components into FreeRTOS project using the MCUXpresso IDE New Project wizard.

# 1.5 ChangeLog

# 1.5.1 MCUXpresso SDK Changelog

# **Board Support Files**

#### board

# [25.06.00]

Initial version

# clock\_config

#### [25.06.00]

• Initial version

# pin\_mux

#### [25.06.00]

• Initial version

# LPC\_ACOMP

#### [2.1.0]

- Bug Fixes
  - Fixed one wrong enum value for the hysteresis.
  - Fixed the violations of MISRA C-2012 rules:
    - \* Rule 10.1, 17.7.

# [2.0.2]

- Bug Fixes
  - Fixed the out-of-bounds error of Coverity caused by missing an assert sentence to avoid the return value of ACOMP\_GetInstance() exceeding the array bounds.

#### [2.0.1]

- New Features
  - Added a control macro to enable/disable the CLOCK code in current driver.

#### [2.0.0]

• Initial version.

#### LPC ADC

# [2.6.0]

- New Features
  - Added new feature macro to distinguish whether the GPADC\_CTRLO\_GPADC\_TSAMP control bit is on the device.
  - Added new variable extendSampleTimeNumber to indicate the ADC extend sample time.
- Bugfix
  - Fixed the bug that incorrectly sets the PASS\_ENABLE bit based on the sample time setting.

#### [2.5.3]

- Improvements
  - Release peripheral from reset if necessary in init function.

#### [2.5.2]

- Improvements
  - Integrated different sequence's sample time numbers into one variable.
- Bug Fixes
  - Fixed violation of MISRA C-2012 rule 20.9.

#### [2.5.1]

- Bug Fixes
  - Fixed ADC conversion sequence priority misconfiguration issue in the ADC\_SetConvSeqAHighPriority() and ADC\_SetConvSeqBHighPriority() APIs.
- Improvements
  - Supported configuration ADC conversion sequence sampling time.

#### [2.5.0]

- Improvements
  - Add missing parameter tag of ADC\_DoOffsetCalibration().
- Bug Fixes
  - Removed a duplicated API with typo in name: ADC\_EnableShresholdCompareInterrupt().

# [2.4.1]

- Bug Fixes
  - Enabled self-calibration after clock divider be changed to make sure the frequency update be taken.

#### [2.4.0]

- New Features
  - Added new API ADC\_DoOffsetCalibration() which supports a specific operation frequency.
- · Other Changes
  - Marked the ADC\_DoSelfCalibration(ADC\_Type \*base) as deprecated.
- Bug Fixes
  - Fixed the violations of MISRA C-2012 rules:
    - \* Rule 10.1 10.3 10.4 10.7 10.8 17.7.

#### [2.3.2]

- Improvements
  - Added delay after enabling using the ADC GPADC\_CTRL0 LDO\_POWER\_EN bit for JN5189/QN9090.
- New Features
  - Added support for platforms which have only one ADC sequence control/result register.

#### [2.3.1]

- Bug Fixes
  - Avoided writing ADC STARTUP register in ADC\_Init().
  - Fixed Coverity zero divider error in ADC\_DoSelfCalibration().

# [2.3.0]

- Improvements
  - Updated "ADC\_Init()""ADC\_GetChannelConversionResult()" API and "adc\_resolution\_t" structure to match QN9090.
  - Added "ADC\_EnableTemperatureSensor" API.

# [2.2.1]

- Improvements
  - Added a brief delay in uSec after ADC calibration start.

# [2.2.0]

- Improvements
  - Updated "ADC\_DoSelfCalibration" API and "adc\_config\_t" structure to match LPC845.

# [2.1.0]

- Improvements
  - Renamed "ADC\_EnableShresholdCompareInterrupt" to "ADC\_EnableThresholdCompareInterrupt".

#### [2.0.0]

• Initial version.

#### **CLOCK**

#### [2.3.4]

- Bug Fixes
  - Fixed violations of MISRA C-2012 rule 11.3.

#### [2.3.3]

- Improvements
  - Added lost comments for some enumerations.

# [2.3.2]

- Improvements
  - Used "offsetof" macro to get the offset of the structure element from the beginning of the structure.

#### [2.3.1]

- Bug Fixes
  - Fixed MISRA C-2012 rule 10.1, rule 10.3, rule 15.5 and so on.

#### [2.3.0]

- New feature:
  - Moved SDK\_DelayAtLeastUs function from clock driver to common driver.

# [2.2.0]

• Replace the delay function

#### [2.1.0]

- New feature
  - Adding new API CLOCK\_DelayAtLeastUs() to implemente a delay fucntion which allow users set delay in unit of microsecond.

# [2.0.3]

- add api to get uart clock frequency.
- add api to set fractional multiplier value.

#### [2.0.2]

• some minor fixes.

# [2.0.0]

• initial version.

#### **COMMON**

# [2.6.0]

- Bug Fixes
  - Fix CERT-C violations.

#### [2.5.0]

- New Features
  - Added new APIs InitCriticalSectionMeasurementContext, DisableGlobalIRQEx and EnableGlobalIRQEx so that user can measure the execution time of the protected sections.

#### [2.4.3]

- Improvements
  - Enable irgs that mount under irgsteer interrupt extender.

#### [2.4.2]

- Improvements
  - Add the macros to convert peripheral address to secure address or non-secure address.

#### [2.4.1]

- Improvements
  - Improve for the macro redefinition error when integrated with zephyr.

#### [2.4.0]

- New Features
  - Added EnableIRQWithPriority, IRQ\_SetPriority, and IRQ\_ClearPendingIRQ for ARM.
  - Added MSDK\_EnableCpuCycleCounter, MSDK\_GetCpuCycleCount for ARM.

# [2.3.3]

- New Features
  - Added NETC into status group.

#### [2.3.2]

- Improvements
  - Make driver aarch64 compatible

# [2.3.1]

- Bug Fixes
  - Fixed MAKE\_VERSION overflow on 16-bit platforms.

# [2.3.0]

- Improvements
  - Split the driver to common part and CPU architecture related part.

# [2.2.10]

- Bug Fixes
  - Fixed the ATOMIC macros build error in cpp files.

#### [2.2.9]

- Bug Fixes
  - Fixed MISRA C-2012 issue, 5.6, 5.8, 8.4, 8.5, 8.6, 10.1, 10.4, 17.7, 21.3.
  - Fixed SDK\_Malloc issue that not allocate memory with required size.

#### [2.2.8]

- Improvements
  - Included stddef.h header file for MDK tool chain.
- New Features:
  - Added atomic modification macros.

# [2.2.7]

- Other Change
  - Added MECC status group definition.

# [2.2.6]

- Other Change
  - Added more status group definition.
- Bug Fixes
  - Undef \_\_VECTOR\_TABLE to avoid duplicate definition in cmsis\_clang.h

# [2.2.5]

- Bug Fixes
  - Fixed MISRA C-2012 rule-15.5.

#### [2.2.4]

- Bug Fixes
  - Fixed MISRA C-2012 rule-10.4.

#### [2.2.3]

- New Features
  - Provided better accuracy of SDK\_DelayAtLeastUs with DWT, use macro SDK\_DELAY\_USE\_DWT to enable this feature.
  - Modified the Cortex-M7 delay count divisor based on latest tests on RT series boards, this setting lets result be closer to actual delay time.

#### [2.2.2]

- New Features
  - Added include RTE\_Components.h for CMSIS pack RTE.

#### [2.2.1]

- Bug Fixes
  - Fixed violation of MISRA C-2012 Rule 3.1, 10.1, 10.3, 10.4, 11.6, 11.9.

#### [2.2.0]

- New Features
  - Moved SDK\_DelayAtLeastUs function from clock driver to common driver.

#### [2.1.4]

- New Features
  - Added OTFAD into status group.

#### [2.1.3]

- Bug Fixes
  - MISRA C-2012 issue fixed.
    - \* Fixed the rule: rule-10.3.

#### [2.1.2]

- Improvements
  - Add SUPPRESS\_FALL\_THROUGH\_WARNING() macro for the usage of suppressing fallthrough warning.

#### [2.1.1]

- Bug Fixes
  - Deleted and optimized repeated macro.

#### [2.1.0]

- New Features
  - Added IRQ operation for XCC toolchain.
  - Added group IDs for newly supported drivers.

#### [2.0.2]

- Bug Fixes
  - MISRA C-2012 issue fixed.
    - \* Fixed the rule: rule-10.4.

#### [2.0.1]

- Improvements
  - Removed the implementation of LPC8XX Enable/DisableDeepSleepIRQ() function.
  - Added new feature macro switch "FSL\_FEATURE\_HAS\_NO\_NONCACHEABLE\_SECTION" for specific SoCs which have no noncacheable sections, that helps avoid an unnecessary complex in link file and the startup file.
  - Updated the align(x) to **attribute**(aligned(x)) to support MDK v6 armclang compiler.

#### [2.0.0]

• Initial version.

#### **CRC**

#### [2.1.1]

• Fix MISRA issue.

# [2.1.0]

• Add CRC\_WriteSeed function.

#### [2.0.2]

• Fix MISRA issue.

#### [2.0.1]

• Fixed KPSDK-13362. MDK compiler issue when writing to WR\_DATA with -O3 optimize for time.

# [2.0.0]

· Initial version.

#### **CTIMER**

# [2.3.3]

- Bug Fixes
  - Fix CERT INT30-C INT31-C issue.
  - Make API CTIMER\_SetupPwm and CTIMER\_UpdatePwmDutycycle return fail if pulse width register overflow.

# [2.3.2]

- Bug Fixes
  - Clear unexpected DMA request generated by RESET\_PeripheralReset in API CTIMER\_Init to avoid trigger DMA by mistake.

# [2.3.1]

- Bug Fixes
  - MISRA C-2012 issue fixed: rule 10.7 and 12.2.

#### [2.3.0]

- Improvements
  - Added the CTIMER\_SetPrescale(), CTIMER\_GetCaptureValue(),
     CTIMER\_EnableResetMatchChannel(),
     CTIMER\_EnableStopMatchChannel(),
     CTIMER\_EnableFallingEdgeCapture(),
     CTIMER\_EnableFallingEdgeCapture(),
     CTIMER\_SetShadowValue(),APIs Interface to reduce code complexity.

#### [2.2.2]

- Bug Fixes
  - Fixed SetupPwm() API only can use match 3 as period channel issue.

# [2.2.1]

- Bug Fixes
  - Fixed use specified channel to setting the PWM period in SetupPwmPeriod() API.
  - Fixed Coverity Out-of-bounds issue.

#### [2.2.0]

- Improvements
  - Updated three API Interface to support Users to flexibly configure the PWM period and PWM output.
- Bug Fixes
  - MISRA C-2012 issue fixed: rule 8.4.

#### [2.1.0]

- Improvements
  - Added the CTIMER\_GetOutputMatchStatus() API Interface.
  - Added feature macro for FSL\_FEATURE\_CTIMER\_HAS\_NO\_CCR\_CAP2 and FSL\_FEATURE\_CTIMER\_HAS\_NO\_IR\_CR2INT.

#### [2.0.3]

- Bug Fixes
  - MISRA C-2012 issue fixed: rule 10.3, 10.4, 10.6, 10.7 and 11.9.

# [2.0.2]

- New Features
  - Added new API "CTIMER\_GetTimerCountValue" to get the current timer count value.
  - Added a control macro to enable/disable the RESET and CLOCK code in current driver.
  - Added a new feature macro to update the API of CTimer driver for lpc8n04.

#### [2.0.1]

- Improvements
  - API Interface Change
    - \* Changed API interface by adding CTIMER\_SetupPwmPeriod API and CTIMER\_UpdatePwmPulsePeriod API, which both can set up the right PWM with high resolution.

# [2.0.0]

• Initial version.

#### **GPIO**

#### [2.1.7]

- Improvements
  - Enhanced GPIO\_PinInit to enable clock internally.

#### [2.1.6]

- Bug Fixes
  - Clear bit before set it within GPIO\_SetPinInterruptConfig() API.

# [2.1.5]

- Bug Fixes
  - Fixed violations of the MISRA C-2012 rules 3.1, 10.6, 10.7, 17.7.

# [2.1.4]

- Improvements
  - Added API GPIO\_PortGetInterruptStatus to retrieve interrupt status for whole port.
  - Corrected typos in header file.

#### [2.1.3]

- Improvements
  - Updated "GPIO\_PinInit" API. If it has DIRCLR and DIRSET registers, use them at set 1 or clean 0.

# [2.1.2]

- Improvements
  - Removed deprecated APIs.

#### [2.1.1]

- Improvements
  - API interface changes:
    - \* Refined naming of APIs while keeping all original APIs, marking them as deprecated. Original APIs will be removed in next release. The mainin change is updating APIs with prefix of \_PinXXX() and \_PorortXXX

#### [2.1.0]

- New Features
  - Added GPIO initialize API.

#### [2.0.0]

· Initial version.

#### I2C

#### [2.2.1]

- Bug Fixes
  - Fixed coverity issues.

#### [2.2.0]

• Removed lpc\_i2c\_dma driver.

# [2.1.0]

- Bug Fixes
  - Fixed MISRA 8.6 violations.

#### [2.0.4]

- Bug Fixes
  - Fixed wrong assignment for datasize in I2C\_InitTransferStateMachineDMA.
  - Fixed wrong working flow in I2C\_RunTransferStateMachineDMA to ensure master can work in no start flag and no stop flag mode.
  - Fixed wrong working flow in I2C\_RunTransferStateMachine and added kReceive-DataBeginState in \_i2c\_transfer\_states to ensure master can work in no start flag and no stop flag mode.
  - Fixed wrong handle state in I2C\_MasterTransferDMAHandleIRQ. After all the data has been transfered or nak is returned, handle state should be changed to idle.
  - Eliminated IAR Pa082 warning in I2C\_SlaveTransferHandleIRQ by assigning volatile variable to local variable and using local variable instead.
  - Fixed MISRA issues.
    - \* Fixed rules 4.7, 10.1, 10.3, 10.4, 11.1, 11.8, 14.4, 17.7.

- Improvements
  - Rounded up the calculated divider value in I2C\_MasterSetBaudRate.
  - Updated the I2C\_WAIT\_TIMEOUT macro to unified name I2C\_RETRY\_TIMES.

#### [2.0.3]

- Bug Fixes
  - Fixed Coverity issue of unchecked return value in I2C RTOS Transfer.

#### [2.0.2]

- New Features
  - Added macro gate "FSL\_SDK\_ENABLE\_I2C\_DRIVER\_TRANSACTIONAL\_APIS" to enable/disable the transactional APIs which will help reduce the code size when no non-blocking transfer is used. Default configuration is enabled.
  - Added a control macro to enable/disable the RESET and CLOCK code in current driver.

# [2.0.1]

- Improvements
  - Added I2C\_WATI\_TIMEOUT macro to allow the user to specify the timeout times for waiting flags in functional API and blocking transfer API.

# [2.0.0]

• Initial version.

#### TAP

#### [2.0.7]

- Bug Fixes
  - Fixed IAP\_ReinvokeISP bug that can't support UART ISP auto baud detection.

#### [2.0.6]

- Bug Fixes
  - Fixed IAP\_ReinvokeISP wrong parameter setting.

#### [2.0.5]

- New Feature
  - Added support config flash memory access time.

#### [2.0.4]

- Bug Fixes
  - Fixed the violations of MISRA 2012 rules 9.1

#### [2.0.3]

- New Features
  - Added support for LPC 845's FAIM operation.
  - Added support for LPC 80x's fixed reference clock for flash controller.
  - Added support for LPC 5411x's Read UID command useless situation.
- Improvements
  - Improved the document and code structure.
- Bug Fixes
  - Fixed the violations of MISRA 2012 rules:
    - \* Rule 10.1 10.3 10.4 17.7

# [2.0.2]

- New Features
  - Added an API to read generated signature.
- Bug Fixes
  - Fixed the incorrect board support of IAP\_ExtendedFlashSignatureRead().

#### [2.0.1]

- New Features
  - Added an API to read factory settings for some calibration registers.
- Improvements
  - Updated the size of result array in part APIs.

#### [2.0.0]

· Initial version.

#### IOCON

# [2.0.2]

- Bug Fixes
  - Fixed MISRA-C 2012 violations.

# [2.0.1]

- Bug Fixes
  - Fixed out-of-range issue of the IOCON mode function when enabling DAC.

#### [2.0.0]

• Initial version.

#### **MRT**

#### [2.0.5]

- Bug Fixes
  - Fixed CERT INT31-C violations.

# [2.0.4]

- Improvements
  - Don't reset MRT when there is not system level MRT reset functions.

#### [2.0.3]

- Bug Fixes
  - Fixed violations of MISRA C-2012 rule 10.1 and 10.4.
  - Fixed the wrong count value assertion in MRT\_StartTimer API.

# [2.0.2]

- Bug Fixes
  - Fixed violations of MISRA C-2012 rule 10.4.

#### [2.0.1]

• Added control macro to enable/disable the RESET and CLOCK code in current driver.

#### [2.0.0]

· Initial version.

#### **PINT**

#### [2.2.0]

- Fixed
  - Fixed the issue that clear interrupt flag when it's not handled. This causes events to be lost.
- Changed
  - Used one callback for one PINT instance. It's unnecessary to provide different callbacks for all PINT events.

#### [2.1.13]

- Improvements
  - Added instance array for PINT to adapt more devices.
  - Used release reset instead of reset PINT which may clear other related registers out of PINT.

#### [2.1.12]

- Bug Fixes
  - Fixed coverity issue.

#### [2.1.11]

- Bug Fixes
  - Fixed MISRA C-2012 rule 10.7 violation.

#### [2.1.10]

- New Features
  - Added the driver support for MCXN10 platform with combined interrupt handler.

#### [2.1.9]

- Bug Fixes
  - Fixed MISRA-2012 rule 8.4.

# [2.1.8]

- Bug Fixes
  - Fixed MISRA-2012 rule 10.1 rule 10.4 rule 10.8 rule 18.1 rule 20.9.

# [2.1.7]

- Improvements
  - Added fully support for the SECPINT, making it can be used just like PINT.

# [2.1.6]

- Bug Fixes
  - Fixed the bug of not enabling common pint clock when enabling security pint clock.

# [2.1.5]

- Bug Fixes
  - Fixed issue for MISRA-2012 check.
    - \* Fixed rule 10.1 rule 10.3 rule 10.4 rule 10.8 rule 14.4.
  - Changed interrupt init order to make pin interrupt configuration more reasonable.

#### [2.1.4]

- Improvements
  - Added feature to control distinguish PINT/SECPINT relevant interrupt/clock configurations for PINT\_Init and PINT\_Deinit API.
  - Swapped the order of clearing PIN interrupt status flag and clearing pending NVIC interrupt in PINT\_EnableCallback and PINT\_EnableCallbackByIndex function.
  - Bug Fixes
    - \* Fixed build issue caused by incorrect macro definitions.

#### [2.1.3]

- Bug fix:
  - Updated PINT\_PinInterruptClrStatus to clear PINT interrupt status when the bit is asserted and check whether was triggered by edge-sensitive mode.
  - Write 1 to IST corresponding bit will clear interrupt status only in edge-sensitive mode and will switch the active level for this pin in level-sensitive mode.
  - Fixed MISRA c-2012 rule 10.1, rule 10.6, rule 10.7.
  - Added FSL\_FEATURE\_SECPINT\_NUMBER\_OF\_CONNECTED\_OUTPUTS to distinguish IRQ relevant array definitions for SECPINT/PINT on lpc55s69 board.
  - Fixed PINT driver c++ build error and remove index offset operation.

#### [2.1.2]

- Improvement:
  - Improved way of initialization for SECPINT/PINT in PINT\_Init API.

#### [2.1.1]

- Improvement:
  - Enabled secure pint interrupt and add secure interrupt handle.

# [2.1.0]

• Added PINT\_EnableCallbackByIndex/PINT\_DisableCallbackByIndex APIs to enable/disable callback by index.

# [2.0.2]

• Added control macro to enable/disable the RESET and CLOCK code in current driver.

# [2.0.1]

- Bug fix:
  - Updated PINT driver to clear interrupt only in Edge sensitive.

#### [2.0.0]

• Initial version.

#### **POWER**

#### [2.1.0]

- New features
  - Added BOD control APIs.

# [2.0.4]

- Bug Fixes
  - Fixed the typo "Enbale", correcting it as "Enable".

# [2.0.3]

- Bug Fixes
  - Fixed doxygen warnings(remove wrong character in annotation).

# [2.0.2]

- New Features
  - Added the Enable/DisableDeepSleepIRQ() to enable/disable pin wake up.

# [2.0.1]

- Improvements
  - Updated power drive to support PMU.

# [2.0.0]

• initial version.

#### **RESET**

#### [2.4.0]

- Improvements
  - Add RESET\_ReleasePeripheralReset API.

# [2.0.1]

• Update component full\_name to "Reset Driver".

#### [2.0.0]

• initial version.

#### **SPI**

#### [2.0.8]

- Bug Fixes
  - Fixed coverity issue.

#### [2.0.7]

- Bug Fixes
  - Fixed the txData from void \* to const void \* in transmit API.

#### [2.0.6]

- Improvements
  - Changed SPI\_DUMMYDATA to 0x00.

# [2.0.5]

- Bug Fixes
  - Fixed bug that the transfer configuration does not take effect after the first transfer.

# [2.0.4]

- Bug Fixes
  - Fixed the issue that when transfer finish callback is invoked TX data is not sent to bus yet.

# [2.0.3]

- Improvements
  - Added timeout mechanism when waiting certain states in transfer driver.
  - Fixed MISRA 10.4 issue.

#### [2.0.2]

- Bug Fixes
  - Fixed Coverity issue of incrementing null pointer in SPI\_MasterTransferNonBlocking.
  - Fixed MISRA issues.
    - \* Fixed rules 10.1, 10.3, 10.4, 10.6, 14.4.
- New Features
  - Added enumeration for dataWidth.

#### [2.0.1]

- Bug Fixes
  - Added wait mechanism in SPI\_MasterTransferBlocking() API, which checks if master SPI becomes IDLE when the EOT bit is set before returning. This confirms that all data will be sent out by SPI master.
  - Fixed the bug that the EOT bit couldn't be set when only one frame was sent in polling mode and interrupt transfer mode.
- New Features
  - Added macro gate "FSL\_SDK\_ENABLE\_SPI\_DRIVER\_TRANSACTIONAL\_APIS" to enable/disable the transactional APIs, which helps reduce the code size when no non-blocking transfer is used. Enabled default configuration.
  - Added a control macro to enable/disable the RESET and CLOCK code in current driver.

# [2.0.0]

• Initial version.

#### **SWM**

#### [2.1.2]

- Improvements
  - Reduce RAM footprint.

#### [2.1.1]

- Bug Fixes
  - MISRA C-2012 issue fixed: rule 10.1 and 10.3.

# [2.1.0]

- New Features
  - Supported Flextimer function pin assign.

#### [2.0.2]

- Bug Fixes
  - MISRA C-2012 issue fixed: rule 14.3.

#### [2.0.1]

- Bug Fixes
  - MISRA C-2012 issue fixed: rule 10.1, 10.3, and 10.4.

# [2.0.0]

- Initial version.
- The API SWM\_SetFixedMovablePinSelect() is targeted at the device that has PINASSIGN-FIXED0 register, such as LPC804.

#### **SYSCON**

# [2.0.1]

- Bug Fixes
  - Fixed issue for MISRA-2012 check.
    - \* Fixed rule 10.4.

# [2.0.0]

· Initial version.

#### **USART**

#### [2.5.2]

- Improvements
  - Fixed coverity issues.

#### [2.5.1]

- Improvements
  - Fixed doxygen warning in USART\_SetRxIdleTimeout.

#### [2.5.0]

- New Features
  - Supported new feature of rx idle timeout.

# [2.4.0]

- Improvements
  - Used separate data for TX and RX in usart\_transfer\_t.
- Bug Fixes
  - Fixed bug that when ring buffer is used, if some data is received in ring buffer first before calling USART\_TransferReceiveNonBlocking, the received data count returned by USART\_TransferGetReceiveCount is wrong.

#### [2.3.0]

- New Features
  - Modified usart\_config\_t, USART\_Init and USART\_GetDefaultConfig APIs so that the hardware flow control can be enabled during module initialization.

#### [2.2.0]

- Improvements
  - Added timeout mechanism when waiting for certain states in transfer driver.
  - Fixed MISRA 10.4 issues.

# [2.1.1]

- Bug Fixes
  - Fixed the bug that in USART\_SetBaudRate best\_diff rather than diff should be used to compare with calculated baudrate.
  - Eliminated IAR pa082 warnings from USART\_TransferGetRxRingBufferLength and USART\_TransferHandleIRQ.
  - Fixed MISRA issues.
- Improvements
  - Rounded up the calculated sbr value in USART\_SetBaudRate to achieve more acurate baudrate setting.
  - Modified USART\_ReadBlocking so that if more than one receiver errors occur, all status flags will be cleared and the most severe error status will be returned.

#### [2.1.0]

- New Features
  - Added new APIs to allow users to configure the USART continuous SCLK feature in synchronous mode transfer.

# [2.0.1]

- Bug Fixes
  - Fixed the repeated reading issue of the STAT register while dealing with the IRQ routine.
- New Features
  - Added macro gate "FSL\_SDK\_ENABLE\_USART\_DRIVER\_TRANSACTIONAL\_APIS" to enable/disable the transactional APIs, which helps reduce the code size when no non-blocking transfer is used. Enabled default configuration.
  - Added a control macro to enable/disable the RESET and CLOCK code in current driver.
  - Added macro switch gate "FSL\_SDK\_USART\_DRIVER\_ENABLE\_BAUDRATE\_AUTO\_GENERATE" to enable/disable the baud rate to generate automatically. Disabling this feature will help reduce the code size to a certain degree. Default configuration enables auto generating of baud rate.
  - Added the check of baud rate while initializing the USART. If the baud rate calculated is not precise, the software assertion will be triggered.

 Added a new API to allow users to enable the CTS, which determines whether CTS is used for flow control.

# [2.0.0]

· Initial version.

#### WKT

#### [2.0.2]

- Bug Fixes
  - Fixed violation of MISRA C-2012 rule 10.3.

# [2.0.1]

- New Features
  - Added control macro to enable/disable the RESET and CLOCK code in current driver.

# [2.0.0]

· Initial version.

#### **WWDT**

#### [2.1.9]

- Bug Fixes
  - Fixed violation of the MISRA C-2012 rule 10.4.

#### [2.1.8]

- Improvements
  - Updated the "WWDT\_Init" API to add wait operation. Which can avoid the TV value read by CPU still be 0xFF (reset value) after WWDT\_Init function returns.

# [2.1.7]

- Bug Fixes
  - Fixed the issue that the watchdog reset event affected the system from PMC.
  - Fixed the issue of setting watchdog WDPROTECT field without considering the backwards compatibility.
  - Fixed the issue of clearing bit fields by mistake in the function of WWDT\_ClearStatusFlags.

#### [2.1.5]

- Bug Fixes
  - deprecated a unusable API in WWWDT driver.
    - \* WWDT Disable

#### [2.1.4]

- Bug Fixes
  - Fixed violation of the MISRA C-2012 rules Rule 10.1, 10.3, 10.4 and 11.9.
  - Fixed the issue of the inseparable process interrupted by other interrupt source.
    - \* WWDT Init

#### [2.1.3]

- Bug Fixes
  - Fixed legacy issue when initializing the MOD register.

#### [2.1.2]

- Improvements
  - Updated the "WWDT\_ClearStatusFlags" API and "WWDT\_GetStatusFlags" API to match QN9090. WDTOF is not set in case of WD reset. Get info from PMC instead.

#### [2.1.1]

- New Features
  - Added new feature definition macro for devices which have no LCOK control bit in MOD register.
  - Implemented delay/retry in WWDT driver.

#### [2.1.0]

- Improvements
  - Added new parameter in configuration when initializing WWDT module. This parameter, which must be set, allows the user to deliver the WWDT clock frequency.

# [2.0.0]

• Initial version.

# 1.6 Driver API Reference Manual

This section provides a link to the Driver API RM, detailing available drivers and their usage to help you integrate hardware efficiently.

LPC802

# 1.7 Middleware Documentation

Find links to detailed middleware documentation for key components. While not all onboard middleware is covered, this serves as a useful reference for configuration and development.

# 1.7.1 FreeMASTER

freemaster

# **Chapter 2**

# **LPC802**

# 2.1 Clock Driver

```
enum _clock_ip_name
     Clock gate name used for CLOCK_EnableClock/CLOCK_DisableClock.
     Values:
    enumerator kCLOCK_IpInvalid
         Invalid Ip Name.
     enumerator kCLOCK_Rom
         Clock gate name: Rom.
    enumerator kCLOCK_Ram0
         Clock gate name: Ram0.
     enumerator kCLOCK_Flash
         Clock gate name: Flash.
    enumerator kCLOCK I2c0
         Clock gate name: I2c0.
     enumerator kCLOCK_Gpio0
         Clock gate name: Gpio0.
    enumerator kCLOCK Swm
         Clock gate name: Swm.
    enumerator \mathrm{kCLOCK}_{-}\mathrm{Wkt}
         Clock gate name: Wkt.
     enumerator kCLOCK_Mrt
         Clock gate name: Mrt.
    enumerator kCLOCK\_Spi0
         Clock gate name: Spi0.
     enumerator kCLOCK_Crc
         Clock gate name: Crc.
     enumerator kCLOCK_Uart0
         Clock gate name: Uart0.
```

```
enumerator kCLOCK_Uart1
         Clock gate name: Uart1.
    enumerator kCLOCK Wwdt
         Clock gate name: Wwdt.
    enumerator kCLOCK_Iocon
         Clock gate name: Iocon.
    enumerator kCLOCK Acmp
         Clock gate name: Acmp.
    enumerator kCLOCK\_Adc
         Clock gate name: Adc.
    enumerator kCLOCK Ctimer0
         Clock gate name: Ctimer0.
    enumerator kCLOCK_GpioInt
        Clock gate name: GpioInt.
enum _clock_name
    Clock name used to get clock frequency.
    Values:
    enumerator kCLOCK CoreSysClk
         Cpu/AHB/AHB matrix/Memories,etc
    enumerator kCLOCK MainClk
        Main clock
    enumerator kCLOCK Fro
        FRO18/24/30
    enumerator kCLOCK FroDiv
        FRO div clock
    enumerator kCLOCK_ExtClk
        External Clock
    enumerator kCLOCK_LPOsc
        Low power Oscillator
    enumerator kCLOCK_Frg
        fractional rate0
enum \_{\rm clock\_select}
    Clock Mux Switches CLK_MUX_DEFINE(reg, mux) reg is used to define the mux register mux
    is used to define the mux value.
    Values:
    enumerator kADC_Clk_From_Fro
        Mux ADC_Clk from Fro.
    enumerator kADC_Clk_From_ClkIn
        Mux ADC_Clk from ClkIn.
    enumerator kUART0_Clk_From_Fro
        Mux UARTO_Clk from Fro.
    enumerator kUART0_Clk_From_MainClk
        Mux UART0_Clk from MainClk.
```

- enumerator kUART0\_Clk\_From\_Frg0Clk Mux UART0\_Clk from Frg0Clk.
- enumerator kUART0\_Clk\_From\_Fro\_Div Mux UART0\_Clk from Fro\_Div.
- enumerator kUART1\_Clk\_From\_Fro Mux UART1\_Clk from Fro.
- enumerator kUART1\_Clk\_From\_MainClk Mux UART1\_Clk from MainClk.
- $\begin{array}{c} \textbf{enumerator} \ \text{kUART1\_Clk\_From\_Frg0Clk} \\ \textbf{Mux} \ \textbf{UART1\_Clk} \ \textbf{from} \ \textbf{Frg0Clk}. \end{array}$
- enumerator kUART1\_Clk\_From\_Fro\_Div Mux UART1\_Clk from Fro\_Div.
- enumerator kI2C\_Clk\_From\_Fro Mux I2C\_Clk from Fro.
- enumerator kI2C\_Clk\_From\_MainClk Mux I2C\_Clk from MainClk.
- enumerator kI2C\_Clk\_From\_Frg0Clk Mux I2C\_Clk from Frg0Clk.
- enumerator kI2C\_Clk\_From\_Fro\_Div Mux I2C\_Clk from Fro\_Div.
- enumerator kSPI\_Clk\_From\_Fro Mux SPI\_Clk from Fro.
- enumerator kSPI\_Clk\_From\_MainClk Mux SPI\_Clk from MainClk.
- enumerator kSPI\_Clk\_From\_Frg0Clk Mux SPI\_Clk from Frg0Clk.
- enumerator kSPI\_Clk\_From\_Fro\_Div Mux SPI\_Clk from Fro\_Div.
- enumerator kFRG0\_Clk\_From\_Fro Mux FRG0\_Clk from Fro.
- enumerator kFRG0\_Clk\_From\_MainClk Mux FRG0\_Clk from MainClk.
- enumerator kCLKOUT\_From\_Fro Mux CLKOUT from Fro.
- enumerator kCLKOUT\_From\_MainClk Mux CLKOUT from MainClk.
- enumerator kCLKOUT\_From\_ExtClk Mux CLKOUT from ExtClk.
- $\begin{array}{c} \textbf{enumerator} \ kCLKOUT\_From\_WdtOsc. \\ \\ \textbf{Mux clock out from WdtOsc.} \end{array}$

enum clock divider

Clock divider.

Values:

2.1. Clock Driver

```
enumerator kCLOCK DivAdcClk
         Adc Clock Divider.
     enumerator kCLOCK DivClkOut
         Clock out divider.
enum clock fro src
     fro output frequency source definition
     Values:
     enumerator kCLOCK FroSrcLpwrBootValue
         fro source from the fro oscillator divided by low power boot value
enum clock fro osc freq
     fro oscillator output frequency value definition
     Values:
     enumerator kCLOCK\_FroOscOut18M
         FRO oscillator output 18M
     enumerator kCLOCK FroOscOut24M
         FRO oscillator output 24M
     enumerator kCLOCK_FroOscOut30M
         FRO oscillator output 30M
enum _clock_main_clk_src
     Main clock source definition.
     Values:
     enumerator kCLOCK_MainClkSrcFro
         main clock source from FRO
     enumerator kCLOCK MainClkSrcExtClk
         main clock source from Ext clock
     enumerator kCLOCK MainClkSrcLPOsc
         main clock source from watchdog oscillator
     enumerator kCLOCK MainClkSrcFroDiv
         main clock source from FRO Div
typedef enum _clock_ip_name clock_ip_name_t
     Clock gate name used for CLOCK EnableClock/CLOCK DisableClock.
typedef enum _clock_name clock_name_t
     Clock name used to get clock frequency.
typedef enum _clock_select clock_select_t
     Clock Mux Switches CLK MUX DEFINE(reg, mux) reg is used to define the mux register mux
     is used to define the mux value.
typedef\ enum\ \_\mathit{clock}\_\mathit{divider}\ \mathrm{clock}\_\mathit{divider}\_t
     Clock divider.
typedef enum _clock_fro_src clock_fro_src_t
     fro output frequency source definition
typedef enum _clock_fro_osc_freq clock_fro_osc_freq_t
     fro oscillator output frequency value definition
```

typedef enum \_clock\_main\_clk\_src clock\_main\_clk\_src\_t

Main clock source definition.

volatile uint $32_t g_Wdt_Osc_Freq$ 

watchdog oscilltor clock frequency.

This variable is used to store the watchdog oscillator frequency which is set by CLOCK InitWdtOsc, and it is returned by CLOCK GetWdtOscFreq.

volatile uint32\_t g\_Ext\_Clk\_Freq

external clock frequency.

This variable is used to store the external clock frequency which is include external oscillator clock and external clk in clock frequency value, it is set by CLOCK\_InitExtClkin when CLK IN is used as external clock or by CLOCK\_InitSysOsc when external oscillator is used as external clock, and it is returned by CLOCK\_GetExtClkFreq.

FSL CLOCK DRIVER VERSION

CLOCK driver version 2.3.4.

SDK\_DEVICE\_MAXIMUM\_CPU\_CLOCK\_FREQUENCY

CLOCK FRO SETTING API ROM ADDRESS

FRO clock setting API address in ROM.

CLOCK FAIM BASE

FAIM base address.

ADC CLOCKS

Clock ip name array for ADC.

ACMP CLOCKS

Clock ip name array for ACMP.

DAC CLOCKS

Clock ip name array for DAC.

SWM CLOCKS

Clock ip name array for SWM.

ROM\_CLOCKS

Clock ip name array for ROM.

 $SRAM\_CLOCKS$ 

Clock ip name array for SRAM.

IOCON\_CLOCKS

Clock ip name array for IOCON.

GPIO\_CLOCKS

Clock ip name array for GPIO.

GPIO\_INT\_CLOCKS

Clock ip name array for GPIO\_INT.

 $DMA\_CLOCKS$ 

Clock ip name array for DMA.

 $CRC\_CLOCKS$ 

Clock ip name array for CRC.

WWDT\_CLOCKS

Clock ip name array for WWDT.

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SCT CLOCKS

Clock ip name array for SCT0.

I2C CLOCKS

Clock ip name array for I2C.

USART\_CLOCKS

Clock ip name array for I2C.

SPI CLOCKS

Clock ip name array for SPI.

CAPT CLOCKS

Clock ip name array for CAPT.

CTIMER CLOCKS

Clock ip name array for CTIMER.

 $MTB\_CLOCKS$ 

Clock ip name array for MTB.

MRT CLOCKS

Clock ip name array for MRT.

WKT\_CLOCKS

Clock ip name array for WKT.

CLK\_GATE\_DEFINE(reg, bit)

Internal used Clock definition only.

 $CLK\_GATE\_GET\_REG(x)$ 

CLK\_GATE\_GET\_BITS\_SHIFT(x)

CLK\_MUX\_DEFINE(reg, mux)

 ${\rm CLK\_MUX\_GET\_REG}(x)$ 

 $CLK\_MUX\_GET\_MUX(x)$ 

CLK\_MAIN\_CLK\_MUX\_DEFINE(preMux, mux)

CLK\_MAIN\_CLK\_MUX\_GET\_PRE\_MUX(x)

 ${\rm CLK\_MAIN\_CLK\_MUX\_GET\_MUX}(x)$ 

CLK\_DIV\_DEFINE(reg)

 $CLK_DIV_GET_REG(x)$ 

CLK\_WDT\_OSC\_DEFINE(freq, regValue)

 $CLK\_WDT\_OSC\_GET\_FREQ(x)$ 

 ${\rm CLK\_WDT\_OSC\_GET\_REG}(x)$ 

 ${\rm CLK\_FRG\_DIV\_REG\_MAP}(base)$ 

CLK\_FRG\_MUL\_REG\_MAP(base)

CLK\_FRG\_SEL\_REG\_MAP(base)

 ${\bf SYS\_AHB\_CLK\_CTRL0}$ 

```
static inline void CLOCK EnableClock(clock_ip_name_t clk)
```

static inline void CLOCK\_DisableClock(clock\_ip\_name\_t clk)

static inline void CLOCK Select(*clock\_select\_t* sel)

static inline void CLOCK\_SetClkDivider(clock\_divider\_t name, uint32\_t value)

static inline uint32\_t CLOCK GetClkDivider(clock\_divider\_t name)

static inline void CLOCK\_SetCoreSysClkDiv(uint32\_t value)

void CLOCK SetMainClkSrc(clock\_main\_clk\_src\_t src)

Set main clock reference source.

#### **Parameters**

• src – Reference clock\_main\_clk\_src\_t to set the main clock source.

static inline void CLOCK SetFRGClkMul(uint32\_t \*base, uint32\_t mul)

 $uint32\_t \ \mathrm{CLOCK\_GetFRGClkFreq}(void)$ 

Return Frequency of FRG0 Clock.

#### Returns

Frequency of FRG0 Clock.

 $uint32\_t CLOCK\_GetMainClkFreq(void)$ 

Return Frequency of Main Clock.

#### **Returns**

Frequency of Main Clock.

uint32\_t CLOCK\_GetFroFreq(void)

Return Frequency of FRO.

#### Returns

Frequency of FRO.

static inline uint32\_t CLOCK GetCoreSysClkFreq(void)

Return Frequency of core.

#### **Returns**

Frequency of core.

uint32\_t CLOCK\_GetClockOutClkFreq(void)

Return Frequency of ClockOut.

#### **Returns**

Frequency of ClockOut

 $uint32\_t \ \mathrm{CLOCK\_GetUart0ClkFreq}(void)$ 

Get UARTO frequency.

# **Return values**

UART0 – frequency value.

uint32\_t CLOCK\_GetUart1ClkFreq(void)

Get UART1 frequency.

# **Return values**

UART1 – frequency value.

2.1. Clock Driver

uint32\_t CLOCK\_GetFreq(clock\_name\_t clockName)

Return Frequency of selected clock.

#### **Returns**

Frequency of selected clock

 $static\ in line\ uint 32\_t\ \mathrm{CLOCK\_GetLPOscFreq}(void)$ 

Get watch dog OSC frequency.

#### **Return values**

watch – dog OSC frequency value.

static inline uint32\_t CLOCK\_GetExtClkFreq(void)

Get external clock frequency.

#### **Return values**

external – clock frequency value.

bool CLOCK\_SetFRGClkFreq(uint32\_t freq)

Set FRG0 output frequency.

#### **Parameters**

 target (freq,) – output frequency,freq < input and (input / freq) < 2 should be satisfy.

#### **Return values**

true – - successfully, false - input argument is invalid.

void CLOCK\_InitExtClkin(uint32\_t clkInFreq)

Init external CLK IN, select the CLKIN as the external clock source.

#### **Parameters**

• clkInFreq – external clock in frequency.

static inline void  $\operatorname{CLOCK\_DeinitLPOsc}(void)$ 

Deinit watch dog OSC.

# **Parameters**

• config – oscillator configuration.

 $void\ \mathrm{CLOCK\_SetFroOscFreq}(\textit{clock\_fro\_osc\_freq\_t}\ freq)$ 

Set FRO oscillator output frequency. Initialize the FRO clock to given frequency (18, 24 or 30 MHz).

#### **Parameters**

• please (freq,) – reference clock\_fro\_osc\_freq\_t definition, frequency must be one of 18000, 24000 or 30000 KHz.

# 2.2 CRC: Cyclic Redundancy Check Driver

FSL CRC DRIVER VERSION

CRC driver version. Version 2.1.1.

Current version: 2.1.1

Change log:

- Version 2.0.0
  - initial version
- Version 2.0.1

- add explicit type cast when writing to WR\_DATA
- Version 2.0.2
  - Fix MISRA issue
- Version 2.1.0
  - Add CRC WriteSeed function
- Version 2.1.1
  - Fix MISRA issue

```
enum crc polynomial
```

CRC polynomials to use.

Values:

```
enumerator kCRC_Polynomial_CRC_CCITT

x^16+x^12+x^5+1

enumerator kCRC_Polynomial_CRC_16
x^16+x^15+x^2+1

enumerator kCRC_Polynomial_CRC_32
x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x+1

typedef enum_crc_polynomial_crc_polynomial_t
CRC polynomials to use.
```

CRC polyholillais to use.

typedef struct \_crc\_config crc\_config\_t

CRC protocol configuration.

This structure holds the configuration for the CRC protocol.

void CRC\_Init(CRC\_Type \*base, const crc\_config\_t \*config)

Enables and configures the CRC peripheral module.

This functions enables the CRC peripheral clock in the LPC SYSCON block. It also configures the CRC engine and starts checksum computation by writing the seed.

### **Parameters**

- base CRC peripheral address.
- config CRC module configuration structure.

static inline void CRC Deinit(CRC Type \*base)

Disables the CRC peripheral module.

This functions disables the CRC peripheral clock in the LPC SYSCON block.

### **Parameters**

• base – CRC peripheral address.

void CRC\_Reset(CRC\_Type \*base)

resets CRC peripheral module.

# **Parameters**

• base – CRC peripheral address.

 $void \ \mathrm{CRC\_WriteSeed}(CRC\_Type \ *base, uint32\_t \ seed)$ 

Write seed to CRC peripheral module.

### **Parameters**

• base – CRC peripheral address.

• seed – CRC Seed value.

void CRC GetDefaultConfig(crc\_config\_t \*config)

Loads default values to CRC protocol configuration structure.

Loads default values to CRC protocol configuration structure. The default values are:

```
config->polynomial = kCRC_Polynomial_CRC_CCITT;
config->reverseIn = false;
config->complementIn = false;
config->reverseOut = false;
config->complementOut = false;
config->seed = 0xFFFFU;
```

#### **Parameters**

• config – CRC protocol configuration structure

```
void CRC_GetConfig(CRC_Type *base, crc_config_t *config)
```

Loads actual values configured in CRC peripheral to CRC protocol configuration structure.

The values, including seed, can be used to resume CRC calculation later.

### **Parameters**

- base CRC peripheral address.
- config CRC protocol configuration structure

void CRC\_WriteData(CRC\_Type \*base, const uint8\_t \*data, size\_t dataSize)

Writes data to the CRC module.

Writes input data buffer bytes to CRC data register.

#### **Parameters**

- base CRC peripheral address.
- data Input data stream, MSByte in data[0].
- dataSize Size of the input data buffer in bytes.

static inline uint32\_t CRC Get32bitResult(CRC\_Type \*base)

Reads 32-bit checksum from the CRC module.

Reads CRC data register.

### **Parameters**

• base – CRC peripheral address.

### **Returns**

final 32-bit checksum, after configured bit reverse and complement operations.

static inline uint16\_t CRC\_Get16bitResult(CRC\_Type \*base)

Reads 16-bit checksum from the CRC module.

Reads CRC data register.

### **Parameters**

• base – CRC peripheral address.

#### Returns

final 16-bit checksum, after configured bit reverse and complement operations.

### CRC\_DRIVER\_USE\_CRC16\_CCITT\_FALSE\_AS\_DEFAULT

Default configuration structure filled by CRC\_GetDefaultConfig(). Uses CRC-16/CCITT-FALSE as default.

```
struct _crc_config
```

#include <fsl crc.h> CRC protocol configuration.

This structure holds the configuration for the CRC protocol.

### **Public Members**

bool reverseIn

Reverse bits on input.

bool complementIn

Perform 1's complement on input.

bool reverseOut

Reverse bits on output.

 $bool\ {\rm complementOut}$ 

Perform 1's complement on output.

 $uint32\_t seed$ 

Starting checksum value.

# 2.3 CTIMER: Standard counter/timers

void CTIMER\_Init(CTIMER\_Type \*base, const *ctimer\_config\_t* \*config)
Ungates the clock and configures the peripheral for basic operation.

**Note:** This API should be called at the beginning of the application before using the driver.

### **Parameters**

- base Ctimer peripheral base address
- config Pointer to the user configuration structure.

void CTIMER Deinit(CTIMER\_Type \*base)

Gates the timer clock.

### **Parameters**

• base – Ctimer peripheral base address

void CTIMER\_GetDefaultConfig(ctimer\_config\_t \*config)

Fills in the timers configuration structure with the default settings.

The default values are:

```
config->mode = kCTIMER_TimerMode;
config->input = kCTIMER_Capture_0;
config->prescale = 0;
```

#### **Parameters**

• config – Pointer to the user configuration structure.

status\_t CTIMER\_SetupPwmPeriod(CTIMER\_Type \*base, const ctimer\_match\_t pwmPeriodChannel, ctimer\_match\_t matchChannel, uint32 t pwmPeriod, uint32 t pulsePeriod, bool enableInt)

Configures the PWM signal parameters.

Enables PWM mode on the match channel passed in and will then setup the match value and other match parameters to generate a PWM signal. This function can manually assign the specified channel to set the PWM cycle.

**Note:** When setting PWM output from multiple output pins, all should use the same PWM period

#### **Parameters**

- $\bullet \ {\rm base}$  Ctimer peripheral base address
- pwmPeriodChannel Specify the channel to control the PWM period
- matchChannel Match pin to be used to output the PWM signal
- pwmPeriod PWM period match value
- pulsePeriod Pulse width match value
- enableInt Enable interrupt when the timer value reaches the match value of the PWM pulse, if it is 0 then no interrupt will be generated.

### Returns

kStatus\_Success on success kStatus\_Fail If matchChannel is equal to pwmPeriodChannel; this channel is reserved to set the PWM cycle If PWM pulse width register value is larger than 0xFFFFFFF.

status\_t CTIMER\_SetupPwm(CTIMER\_Type \*base, const ctimer\_match\_t pwmPeriodChannel, ctimer\_match\_t matchChannel, uint8\_t dutyCyclePercent, uint32\_t pwmFreq\_Hz, uint32\_t srcClock\_Hz, bool enableInt)

Configures the PWM signal parameters.

Enables PWM mode on the match channel passed in and will then setup the match value and other match parameters to generate a PWM signal. This function can manually assign the specified channel to set the PWM cycle.

**Note:** When setting PWM output from multiple output pins, all should use the same PWM frequency. Please use CTIMER\_SetupPwmPeriod to set up the PWM with high resolution.

### **Parameters**

- base Ctimer peripheral base address
- pwmPeriodChannel Specify the channel to control the PWM period
- $\bullet \; \operatorname{matchChannel} Match \; pin \; to \; be \; used \; to \; output \; the \; PWM \; signal$
- dutyCyclePercent PWM pulse width; the value should be between 0 to 100
- pwmFreq\_Hz PWM signal frequency in Hz
- $srcClock\_Hz$  Timer counter clock in Hz
- enableInt Enable interrupt when the timer value reaches the match value of the PWM pulse, if it is 0 then no interrupt will be generated.

static inline void CTIMER\_UpdatePwmPulsePeriod(CTIMER\_Type \*base, ctimer\_match\_t matchChannel, uint32\_t pulsePeriod)

Updates the pulse period of an active PWM signal.

### **Parameters**

- base Ctimer peripheral base address
- matchChannel Match pin to be used to output the PWM signal
- pulsePeriod New PWM pulse width match value

Updates the duty cycle of an active PWM signal.

**Note:** Please use CTIMER\_SetupPwmPeriod to update the PWM with high resolution. This function can manually assign the specified channel to set the PWM cycle.

#### **Parameters**

- base Ctimer peripheral base address
- pwmPeriodChannel Specify the channel to control the PWM period
- matchChannel Match pin to be used to output the PWM signal
- $\operatorname{dutyCyclePercent}$  New PWM pulse width; the value should be between 0 to 100

#### **Returns**

kStatus\_Success on success kStatus\_Fail If PWM pulse width register value is larger than 0xFFFFFFF.

static inline void CTIMER\_EnableInterrupts(CTIMER\_Type \*base, uint32\_t mask) Enables the selected Timer interrupts.

### **Parameters**

- base Ctimer peripheral base address
- mask The interrupts to enable. This is a logical OR of members of the enumeration ctimer\_interrupt\_enable\_t

static inline void CTIMER\_DisableInterrupts(CTIMER\_Type \*base, uint32\_t mask) Disables the selected Timer interrupts.

### **Parameters**

- base Ctimer peripheral base address
- $\bullet \ {\rm mask}$  The interrupts to enable. This is a logical OR of members of the enumeration ctimer\_interrupt\_enable\_t

 $static\ in line\ uint 32\_t\ \mathrm{CTIMER\_GetEnabledInterrupts}(CTIMER\_Type\ *base)$ 

Gets the enabled Timer interrupts.

### **Parameters**

• base – Ctimer peripheral base address

### Returns

The enabled interrupts. This is the logical OR of members of the enumeration ctimer interrupt enable t

```
static inline uint32_t \operatorname{CTIMER\_GetStatusFlags}(\operatorname{CTIMER\_Type *base}) Gets the Timer status flags.
```

### **Parameters**

• base – Ctimer peripheral base address

### **Returns**

The status flags. This is the logical OR of members of the enumeration ctimer\_status\_flags\_t

 $static\ in line\ void\ \mathrm{CTIMER\_ClearStatusFlags}(CTIMER\_Type\ *base,\ uint 32\_t\ mask)$ 

Clears the Timer status flags.

### **Parameters**

- base Ctimer peripheral base address
- mask The status flags to clear. This is a logical OR of members of the enumeration ctimer\_status\_flags\_t

static inline void CTIMER\_StartTimer(CTIMER\_Type \*base)

Starts the Timer counter.

#### **Parameters**

• base – Ctimer peripheral base address

static inline void CTIMER\_StopTimer(CTIMER\_Type \*base)

Stops the Timer counter.

#### **Parameters**

• base – Ctimer peripheral base address

```
{\tt FSL\_CTIMER\_DRIVER\_VERSION}
```

Version 2.3.3

 $enum\_ctimer\_capture\_channel$ 

List of Timer capture channels.

Values:

enumerator kCTIMER\_Capture\_0

Timer capture channel 0

enumerator kCTIMER\_Capture\_1

Timer capture channel 1

enumerator kCTIMER\_Capture\_3

Timer capture channel 3

enum \_ctimer\_capture\_edge

List of capture edge options.

Values:

enumerator kCTIMER\_Capture\_RiseEdge

Capture on rising edge

 $enumerator \ kCTIMER\_Capture\_FallEdge$ 

Capture on falling edge

 $enumerator \ kCTIMER\_Capture\_BothEdge$ 

Capture on rising and falling edge

```
enum _ctimer_match
    List of Timer match registers.
    Values:
    enumerator kCTIMER Match 0
        Timer match register 0
    enumerator kCTIMER Match 1
        Timer match register 1
    enumerator kCTIMER_Match_2
        Timer match register 2
    enumerator kCTIMER_Match_3
        Timer match register 3
enum ctimer external match
    List of external match.
    Values:
    enumerator kCTIMER External Match 0
        External match 0
    enumerator kCTIMER_External_Match_1
        External match 1
    enumerator kCTIMER_External_Match_2
        External match 2
    enumerator kCTIMER_External_Match_3
        External match 3
enum ctimer match output control
    List of output control options.
    Values:
    enumerator kCTIMER_Output_NoAction
        No action is taken
    enumerator kCTIMER Output Clear
         Clear the EM bit/output to 0
    enumerator kCTIMER_Output_Set
         Set the EM bit/output to 1
    enumerator kCTIMER_Output_Toggle
        Toggle the EM bit/output
enum ctimer timer mode
    List of Timer modes.
    Values:
    enumerator kCTIMER TimerMode
    enumerator \ kCTIMER\_IncreaseOnRiseEdge
    enumerator kCTIMER IncreaseOnFallEdge
    enumerator kCTIMER IncreaseOnBothEdge
```

```
enum \_ ctimer\_ interrupt\_ enable
     List of Timer interrupts.
     Values:
     enumerator kCTIMER Match0InterruptEnable
         Match 0 interrupt
     enumerator kCTIMER Match1InterruptEnable
         Match 1 interrupt
     enumerator kCTIMER Match2InterruptEnable
         Match 2 interrupt
     enumerator kCTIMER Match3InterruptEnable
         Match 3 interrupt
enum ctimer status flags
     List of Timer flags.
     Values:
     enumerator kCTIMER Match0Flag
         Match 0 interrupt flag
     enumerator kCTIMER_Match1Flag
          Match 1 interrupt flag
     enumerator kCTIMER_Match2Flag
          Match 2 interrupt flag
     enumerator kCTIMER_Match3Flag
         Match 3 interrupt flag
enum ctimer callback type t
     Callback type when registering for a callback. When registering a callback an array of
     function pointers is passed the size could be 1 or 8, the callback type will tell that.
     Values:
     enumerator \ kCTIMER\_SingleCallback
          Single Callback type where there is only one callback for the timer. based on the status
          flags different channels needs to be handled differently
     enumerator kCTIMER MultipleCallback
          Multiple Callback type where there can be 8 valid callbacks, one per channel. for both
         match/capture
typedef enum _ctimer_capture_channel ctimer_capture_channel_t
     List of Timer capture channels.
typedef enum _ctimer_capture_edge ctimer_capture_edge_t
     List of capture edge options.
typedef\ enum\ \_\mathit{ctimer}\_\mathit{match}\ \mathrm{ctimer}\_\mathit{match}\_t
     List of Timer match registers.
typedef\ enum\ \_ctimer\_external\_match\ {\it ctimer}\_external\_match\_t
     List of external match.
typedef enum _ctimer_match_output_control ctimer_match_output_control_t
     List of output control options.
```

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typedef enum \_ctimer\_timer\_mode ctimer\_timer\_mode\_t

List of Timer modes.

 $typedef\ enum\ \_ctimer\_interrupt\_enable\ {\tt ctimer}\_interrupt\_enable\ \_{\tt t}$ 

List of Timer interrupts.

typedef enum \_ctimer\_status\_flags ctimer\_status\_flags\_t

List of Timer flags.

typedef void (\*ctimer\_callback\_t)(uint32\_t flags)

 $typedef\ struct\_\mathit{ctimer}\_\mathit{match}\_\mathit{config}\ \mathrm{ctimer}\_\mathit{match}\_\mathit{config}\_t$ 

Match configuration.

This structure holds the configuration settings for each match register.

typedef struct \_ctimer\_config ctimer config t

Timer configuration structure.

This structure holds the configuration settings for the Timer peripheral. To initialize this structure to reasonable defaults, call the CTIMER\_GetDefaultConfig() function and pass a pointer to the configuration structure instance.

The configuration structure can be made constant so as to reside in flash.

void CTIMER\_SetupMatch(CTIMER\_Type \*base, ctimer\_match\_t matchChannel, const ctimer match config t \*config)

Setup the match register.

User configuration is used to setup the match value and action to be taken when a match occurs.

#### **Parameters**

- base Ctimer peripheral base address
- matchChannel Match register to configure
- config Pointer to the match configuration structure

 $uint 32\_t \ \mathrm{CTIMER\_GetOutputMatchStatus}(CTIMER\_Type \ *base, \ uint 32\_t \ matchChannel)$ 

Get the status of output match.

This function gets the status of output MAT, whether or not this output is connected to a pin. This status is driven to the MAT pins if the match function is selected via IOCON. 0 = LOW. 1 = HIGH.

### **Parameters**

- base Ctimer peripheral base address
- matchChannel External match channel, user can obtain the status of multiple match channels at the same time by using the logic of "|" enumeration ctimer\_external\_match\_t

# Returns

The mask of external match channel status flags. Users need to use the \_ctimer\_external\_match type to decode the return variables.

void CTIMER\_SetupCapture(CTIMER\_Type \*base, ctimer\_capture\_channel\_t capture, ctimer\_capture edge t edge, bool enableInt)

Setup the capture.

### **Parameters**

- base Ctimer peripheral base address
- capture Capture channel to configure

- edge Edge on the channel that will trigger a capture
- enableInt Flag to enable channel interrupts, if enabled then the registered call back is called upon capture

static inline uint32\_t CTIMER\_GetTimerCountValue(CTIMER\_Type \*base)

Get the timer count value from TC register.

### **Parameters**

• base – Ctimer peripheral base address.

#### **Returns**

return the timer count value.

void CTIMER\_RegisterCallBack(CTIMER\_Type \*base, ctimer\_callback\_t \*cb\_func, ctimer\_callback\_type\_t cb\_type)

Register callback.

This function configures CTimer Callback in following modes:

- Single Callback: cb\_func should be pointer to callback function pointer For example: ctimer\_callback\_t ctimer\_callback = pwm\_match\_callback; CTIMER\_RegisterCallBack(CTIMER, &ctimer\_callback, kCTIMER\_SingleCallback);
- Multiple Callback: cb\_func should be pointer to array of callback function pointers Each element corresponds to Interrupt Flag in IR register. For example: ctimer\_callback\_t ctimer\_callback\_table[] = { ctimer\_match0\_callback, NULL, NULL, ctimer\_match3\_callback, NULL, NULL, NULL, NULL, NULL}; CTIMER\_RegisterCallBack(CTIMER, &ctimer\_callback\_table[0], kC-TIMER\_MultipleCallback);

### **Parameters**

- base Ctimer peripheral base address
- cb\_func Pointer to callback function pointer
- cb type callback function type, singular or multiple

static inline void CTIMER\_Reset(CTIMER\_Type \*base)

Reset the counter.

The timer counter and prescale counter are reset on the next positive edge of the APB clock.

#### **Parameters**

• base – Ctimer peripheral base address

static inline void CTIMER SetPrescale(CTIMER\_Type \*base, uint32\_t prescale)

Setup the timer prescale value.

Specifies the maximum value for the Prescale Counter.

### **Parameters**

- base Ctimer peripheral base address
- prescale Prescale value

static inline uint 32\_t CTIMER\_GetCaptureValue(CTIMER\_Type \*base,  $ctimer\_capture\_channel\_t$  capture)

Get capture channel value.

Get the counter/timer value on the corresponding capture channel.

#### **Parameters**

• base – Ctimer peripheral base address

• capture - Select capture channel

#### **Returns**

The timer count capture value.

static inline void CTIMER\_EnableResetMatchChannel(CTIMER\_Type \*base, ctimer\_match\_t match, bool enable)

Enable reset match channel.

Set the specified match channel reset operation.

### **Parameters**

- base Ctimer peripheral base address
- match match channel used
- enable Enable match channel reset operation.

static inline void CTIMER\_EnableStopMatchChannel(CTIMER\_Type \*base, ctimer\_match\_t match, bool enable)

Enable stop match channel.

Set the specified match channel stop operation.

#### **Parameters**

- base Ctimer peripheral base address.
- match match channel used.
- enable Enable match channel stop operation.

static inline void CTIMER\_EnableMatchChannelReload(CTIMER\_Type \*base, ctimer\_match\_t match, bool enable)

Enable reload channel falling edge.

Enable the specified match channel reload match shadow value.

#### **Parameters**

- base Ctimer peripheral base address.
- match match channel used.
- enable Enable.

static inline void CTIMER\_EnableRisingEdgeCapture(CTIMER\_Type \*base,

ctimer\_capture\_channel\_t capture, bool
enable)

Enable capture channel rising edge.

Sets the specified capture channel for rising edge capture.

#### **Parameters**

- base Ctimer peripheral base address.
- capture capture channel used.
- enable Enable rising edge capture.

static inline void CTIMER\_EnableFallingEdgeCapture(CTIMER\_Type \*base,

ctimer\_capture\_channel\_t capture, bool
enable)

Enable capture channel falling edge.

Sets the specified capture channel for falling edge capture.

### **Parameters**

- base Ctimer peripheral base address.
- capture capture channel used.
- enable Enable falling edge capture.

static inline void CTIMER\_SetShadowValue(CTIMER\_Type \*base, ctimer\_match\_t match, uint32 t matchvalue)

Set the specified match shadow channel.

#### **Parameters**

- base Ctimer peripheral base address.
- match match channel used.
- matchvalue Reload the value of the corresponding match register.

struct ctimer match config

#include <fsl\_ctimer.h> Match configuration.

This structure holds the configuration settings for each match register.

#### **Public Members**

 $uint32_t$  matchValue

This is stored in the match register

bool enableCounterReset

true: Match will reset the counter false: Match will not reser the counter

bool enableCounterStop

true: Match will stop the counter false: Match will not stop the counter

ctimer\_match\_output\_control\_t outControl

Action to be taken on a match on the EM bit/output

bool outPinInitState

Initial value of the EM bit/output

bool enableInterrupt

true: Generate interrupt upon match false: Do not generate interrupt on match

struct \_ctimer\_config

#include <fsl\_ctimer.h> Timer configuration structure.

This structure holds the configuration settings for the Timer peripheral. To initialize this structure to reasonable defaults, call the CTIMER\_GetDefaultConfig() function and pass a pointer to the configuration structure instance.

The configuration structure can be made constant so as to reside in flash.

#### **Public Members**

ctimer timer mode t mode

Timer mode

ctimer capture channel t input

Input channel to increment the timer, used only in timer modes that rely on this input signal to increment TC

uint32\_t prescale

Prescale value

# 2.4 I2C: Inter-Integrated Circuit Driver

# 2.5 I2C Driver

```
FSL_I2C_DRIVER_VERSION I2C driver version.
```

I2C status return codes.

Values:

enumerator kStatus\_I2C\_Busy

The master is already performing a transfer.

enumerator kStatus I2C Idle

The slave driver is idle.

enumerator kStatus\_I2C\_Nak

The slave device sent a NAK in response to a byte.

enumerator kStatus I2C InvalidParameter

Unable to proceed due to invalid parameter.

enumerator kStatus I2C BitError

Transferred bit was not seen on the bus.

enumerator kStatus I2C ArbitrationLost

Arbitration lost error.

 $enumerator \ kStatus\_I2C\_NoTransferInProgress$ 

Attempt to abort a transfer when one is not in progress.

enumerator kStatus\_I2C\_DmaRequestFail

DMA request failed.

enumerator kStatus\_I2C\_StartStopError

Start and stop error.

 $enumerator \ kStatus\_I2C\_UnexpectedState$ 

Unexpected state.

enumerator kStatus\_I2C\_Addr\_Nak

NAK received during the address probe.

enumerator kStatus\_I2C\_Timeout

Timeout polling status flags.

I2C\_RETRY\_TIMES

Retry times for waiting flag.

I2C\_STAT\_MSTCODE\_IDLE

Master Idle State Code

I2C\_STAT\_MSTCODE\_RXREADY

Master Receive Ready State Code

I2C\_STAT\_MSTCODE\_TXREADY

Master Transmit Ready State Code

```
I2C_STAT_MSTCODE_NACKADR

Master NACK by slave on address State Code

I2C_STAT_MSTCODE_NACKDAT

Master NACK by slave on data State Code

I2C_STAT_SLVST_ADDR

I2C_STAT_SLVST_RX

I2C_STAT_SLVST_TX
```

# 2.6 I2C Master Driver

void I2C\_MasterGetDefaultConfig(i2c\_master\_config\_t \*masterConfig)

Provides a default configuration for the I2C master peripheral.

This function provides the following default configuration for the I2C master peripheral:

```
\begin{array}{ll} {\rm masterConfig\text{-}}{\rm enableMaster} & = {\rm true}; \\ {\rm masterConfig\text{-}}{\rm >}{\rm baudRate\_Bps} & = 100000{\rm U}; \\ {\rm masterConfig\text{-}}{\rm >}{\rm enableTimeout} & = {\rm false}; \end{array}
```

After calling this function, you can override any settings in order to customize the configuration, prior to initializing the master driver with I2C\_MasterInit().

#### **Parameters**

masterConfig – [out] User provided configuration structure for default values. Refer to i2c\_master\_config\_t.

```
\label{local_master_local_master_local} \begin{tabular}{ll} void $I2C\_MasterInit(I2C\_Type *base, const $i2c\_master\_config\_t *masterConfig, uint32\_t srcClock\_Hz) \end{tabular}
```

Initializes the I2C master peripheral.

This function enables the peripheral clock and initializes the I2C master peripheral as described by the user provided configuration. A software reset is performed prior to configuration.

### **Parameters**

- $\bullet \ {\rm base}$  The I2C peripheral base address.
- masterConfig User provided peripheral configuration. Use I2C\_MasterGetDefaultConfig() to get a set of defaults that you can override.
- srcClock\_Hz Frequency in Hertz of the I2C functional clock. Used to calculate the baud rate divisors, filter widths, and timeout periods.

void I2C\_MasterDeinit(I2C\_Type \*base)

Deinitializes the I2C master peripheral.

This function disables the I2C master peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

### **Parameters**

• base – The I2C peripheral base address.

uint32\_t I2C\_GetInstance(I2C\_Type \*base)

Returns an instance number given a base address.

If an invalid base address is passed, debug builds will assert. Release builds will just return instance number 0.

#### **Parameters**

• base – The I2C peripheral base address.

#### Returns

I2C instance number starting from 0.

static inline void I2C\_MasterReset(I2C\_Type \*base)

Performs a software reset.

Restores the I2C master peripheral to reset conditions.

### **Parameters**

• base – The I2C peripheral base address.

static inline void I2C\_MasterEnable(I2C\_Type \*base, bool enable)

Enables or disables the I2C module as master.

### **Parameters**

- $\bullet \ {\rm base}$  The I2C peripheral base address.
- enable Pass true to enable or false to disable the specified I2C as master.

static inline uint32\_t I2C\_GetStatusFlags(I2C\_Type \*base)

Gets the I2C status flags.

A bit mask with the state of all I2C status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

### See also:

\_i2c\_master\_flags

### **Parameters**

• base – The I2C peripheral base address.

# Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

static inline void I2C\_MasterClearStatusFlags(I2C\_Type \*base, uint32\_t statusMask)

Clears the I2C master status flag state.

The following status register flags can be cleared:

- kI2C MasterArbitrationLostFlag
- kI2C\_MasterStartStopErrorFlag

Attempts to clear other flags has no effect.

### See also:

\_i2c\_master\_flags.

#### **Parameters**

- base The I2C peripheral base address.
- statusMask A bitmask of status flags that are to be cleared. The mask is composed of \_i2c\_master\_flags enumerators OR'd together. You may pass the result of a previous call to I2C\_GetStatusFlags().

 $static\ in line\ void\ {\tt I2C\_EnableInterrupts} (I2C\_Type\ *base,\ uint 32\_t\ interrupt Mask)$ 

Enables the I2C master interrupt requests.

#### **Parameters**

- base The I2C peripheral base address.
- interruptMask Bit mask of interrupts to enable. See \_i2c\_master\_flags for the set of constants that should be OR'd together to form the bit mask.

static inline void I2C\_DisableInterrupts(I2C\_Type \*base, uint32\_t interruptMask)

Disables the I2C master interrupt requests.

### **Parameters**

- base The I2C peripheral base address.
- interruptMask Bit mask of interrupts to disable. See \_i2c\_master\_flags for the set of constants that should be OR'd together to form the bit mask.

static inline uint32\_t I2C\_GetEnabledInterrupts(I2C\_Type \*base)

Returns the set of currently enabled I2C master interrupt requests.

#### **Parameters**

• base – The I2C peripheral base address.

### **Returns**

A bitmask composed of \_i2c\_master\_flags enumerators OR'd together to indicate the set of enabled interrupts.

 $void\ {\tt I2C\_MasterSetBaudRate} (I2C\_Type\ *base,\ uint32\_t\ baudRate\_Bps,\ uint32\_t\ srcClock\_Hz)\\ Sets\ the\ {\tt I2C}\ bus\ frequency\ for\ master\ transactions.$ 

The I2C master is automatically disabled and re-enabled as necessary to configure the baud rate. Do not call this function during a transfer, or the transfer is aborted.

#### **Parameters**

- base The I2C peripheral base address.
- srcClock\_Hz I2C functional clock frequency in Hertz.
- baudRate Bps Requested bus frequency in bits per second.

static inline bool I2C MasterGetBusIdleState(I2C Type \*base)

Returns whether the bus is idle.

Requires the master mode to be enabled.

#### **Parameters**

• base – The I2C peripheral base address.

### **Return values**

- true Bus is busy.
- false Bus is idle.

status\_t I2C\_MasterStart(I2C\_Type \*base, uint8\_t address, i2c\_direction\_t direction)
Sends a START on the I2C bus.

This function is used to initiate a new master mode transfer by sending the START signal. The slave address is sent following the I2C START signal.

#### **Parameters**

- base I2C peripheral base pointer
- address 7-bit slave device address.
- direction Master transfer directions(transmit/receive).

# **Return values**

- kStatus Success Successfully send the start signal.
- kStatus I2C Busy Current bus is busy.

status\_t I2C MasterStop(I2C\_Type \*base)

Sends a STOP signal on the I2C bus.

### **Return values**

- kStatus\_Success Successfully send the stop signal.
- kStatus\_I2C\_Timeout Send stop signal failed, timeout.

static inline  $status\_t$  I2C\_MasterRepeatedStart(I2C\_Type \*base, uint8\_t address,  $i2c\_direction\_t$  direction)

Sends a REPEATED START on the I2C bus.

#### **Parameters**

- base I2C peripheral base pointer
- address 7-bit slave device address.
- direction Master transfer directions(transmit/receive).

#### **Return values**

- kStatus\_Success Successfully send the start signal.
- kStatus\_I2C\_Busy Current bus is busy but not occupied by current I2C master.

status\_t I2C\_MasterWriteBlocking(I2C\_Type \*base, const void \*txBuff, size\_t txSize, uint32\_t flags)

Performs a polling send transfer on the I2C bus.

Sends up to *txSize* number of bytes to the previously addressed slave device. The slave may reply with a NAK to any byte in order to terminate the transfer early. If this happens, this function returns kStatus\_I2C\_Nak.

# **Parameters**

- base The I2C peripheral base address.
- txBuff The pointer to the data to be transferred.
- ${\rm txSize}$  The length in bytes of the data to be transferred.
- ${
  m flags}$  Transfer control flag to control special behavior like suppressing start or stop, for normal transfers use kI2C\_TransferDefaultFlag

### **Return values**

- kStatus Success Data was sent successfully.
- kStatus\_I2C\_Busy Another master is currently utilizing the bus.

- kStatus I2C Nak The slave device sent a NAK in response to a byte.
- kStatus I2C ArbitrationLost Arbitration lost error.

status\_t I2C\_MasterReadBlocking(I2C\_Type \*base, void \*rxBuff, size\_t rxSize, uint32\_t flags)
Performs a polling receive transfer on the I2C bus.

### **Parameters**

- base The I2C peripheral base address.
- rxBuff The pointer to the data to be transferred.
- rxSize The length in bytes of the data to be transferred.
- flags Transfer control flag to control special behavior like suppressing start or stop, for normal transfers use kI2C\_TransferDefaultFlag

#### **Return values**

- kStatus\_Success Data was received successfully.
- $\bullet~{\rm kStatus\_I2C\_Busy}$  Another master is currently utilizing the bus.
- kStatus\_I2C\_Nak The slave device sent a NAK in response to a byte.
- kStatus\_I2C\_ArbitrationLost Arbitration lost error.

status\_t I2C\_MasterTransferBlocking(I2C\_Type \*base, i2c\_master\_transfer\_t \*xfer)
Performs a master polling transfer on the I2C bus.

**Note:** The API does not return until the transfer succeeds or fails due to arbitration lost or receiving a NAK.

### **Parameters**

- base I2C peripheral base address.
- xfer Pointer to the transfer structure.

### **Return values**

- kStatus Success Successfully complete the data transmission.
- kStatus I2C Busy Previous transmission still not finished.
- kStatus I2C Timeout Transfer error, wait signal timeout.
- kStatus I2C ArbitrationLost Transfer error, arbitration lost.
- kStataus\_I2C\_Nak Transfer error, receive NAK during transfer.

 $\label{local_master_transfer} \begin{tabular}{l} void I2C\_MasterTransferCreateHandle(I2C\_Type *base, i2c\_master\_handle\_t *handle, i2c\_master\_transfer\_callback\_t callback, void *userData) \\ \end{tabular}$ 

Creates a new handle for the I2C master non-blocking APIs.

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the I2C\_MasterTransferAbort() API shall be called.

### **Parameters**

- base The I2C peripheral base address.
- handle [out] Pointer to the I2C master driver handle.
- $\operatorname{callback}$  User provided pointer to the asynchronous callback function.
- userData User provided pointer to the application callback data.

 $status\_t \ I2C\_Master Transfer NonBlocking (I2C\_Type *base, i2c\_master\_handle\_t *handle, i2c\_master\_transfer\_t *xfer)$ 

Performs a non-blocking transaction on the I2C bus.

#### **Parameters**

- base The I2C peripheral base address.
- handle Pointer to the I2C master driver handle.
- xfer The pointer to the transfer descriptor.

#### **Return values**

- kStatus Success The transaction was started successfully.
- kStatus\_I2C\_Busy Either another master is currently utilizing the bus, or a non-blocking transaction is already in progress.

 $status\_t$  I2C\_MasterTransferGetCount(I2C\_Type \*base,  $i2c\_master\_handle\_t$  \*handle, size\_t \*count)

Returns number of bytes transferred so far.

#### **Parameters**

- base The I2C peripheral base address.
- handle Pointer to the I2C master driver handle.
- count **[out]** Number of bytes transferred so far by the non-blocking transaction.

### **Return values**

- kStatus Success -
- kStatus I2C Busy –

status\_t I2C MasterTransferAbort(I2C\_Type \*base, i2c\_master\_handle\_t \*handle)

Terminates a non-blocking I2C master transmission early.

**Note:** It is not safe to call this function from an IRQ handler that has a higher priority than the I2C peripheral's IRQ priority.

### **Parameters**

- base The I2C peripheral base address.
- handle Pointer to the I2C master driver handle.

## **Return values**

- kStatus Success A transaction was successfully aborted.
- kStatus\_I2C\_Timeout Abort failure due to flags polling timeout.

void I2C MasterTransferHandleIRQ(I2C\_Type \*base, void \*i2cHandle)

Reusable routine to handle master interrupts.

**Note:** This function does not need to be called unless you are reimplementing the non-blocking API's interrupt handler routines to add special functionality.

#### **Parameters**

• base – The I2C peripheral base address.

```
    i2cHandle – Pointer to the I2C master driver handle i2c_master_handle_t.

enum i2c master flags
     I2C master peripheral flags.
     Note: These enums are meant to be OR'd together to form a bit mask.
     Values:
     enumerator kI2C_MasterPendingFlag
         The I2C module is waiting for software interaction.
     enumerator kI2C MasterArbitrationLostFlag
         The arbitration of the bus was lost. There was collision on the bus
     enumerator kI2C MasterStartStopErrorFlag
         There was an error during start or stop phase of the transaction.
enum i2c direction
     Direction of master and slave transfers.
     Values:
     enumerator kI2C Write
         Master transmit.
     enumerator kI2C Read
         Master receive.
enum _i2c_master_transfer_flags
     Transfer option flags.
     Note: These enumerations are intended to be OR'd together to form a bit mask of options
     for the _i2c_master_transfer::flags field.
     Values:
     enumerator kI2C TransferDefaultFlag
         Transfer starts with a start signal, stops with a stop signal.
     enumerator kI2C_TransferNoStartFlag
         Don't send a start condition, address, and sub address
     enumerator kI2C TransferRepeatedStartFlag
         Send a repeated start condition
     enumerator kI2C TransferNoStopFlag
         Don't send a stop condition.
enum i2c transfer states
     States for the state machine used by transactional APIs.
     Values:
     enumerator kIdleState
     enumerator kTransmitSubaddrState
     enumerator kTransmitDataState
     enumerator kReceiveDataBeginState
```

enumerator kReceiveDataState

enumerator kReceiveLastDataState

enumerator kStartState

enumerator kStopState

enumerator kWaitForCompletionState

typedef enum i2c direction i2c direction t

Direction of master and slave transfers.

typedef struct \_i2c\_master\_config i2c\_master\_config\_t

Structure with settings to initialize the I2C master module.

This structure holds configuration settings for the I2C peripheral. To initialize this structure to reasonable defaults, call the I2C\_MasterGetDefaultConfig() function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

typedef struct \_i2c\_master\_transfer i2c\_master\_transfer\_t

I2C master transfer typedef.

 $typedef\ struct\ \_i2c\_master\_handle\ i2c\_master\_handle\_t$ 

I2C master handle typedef.

typedef void (\*i2c\_master\_transfer\_callback\_t)(I2C\_Type \*base, *i2c\_master\_handle\_t* \*handle, *status\_t* completionStatus, void \*userData)

Master completion callback function pointer type.

This callback is used only for the non-blocking master transfer API. Specify the callback you wish to use in the call to I2C\_MasterTransferCreateHandle().

#### Param base

The I2C peripheral base address.

### Param completionStatus

Either kStatus\_Success or an error code describing how the transfer completed.

### Param userData

Arbitrary pointer-sized value passed from the application.

```
struct _i2c_master_config
```

#include <fsl\_i2c.h> Structure with settings to initialize the I2C master module.

This structure holds configuration settings for the I2C peripheral. To initialize this structure to reasonable defaults, call the I2C\_MasterGetDefaultConfig() function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

### **Public Members**

bool enableMaster

Whether to enable master mode.

uint32\_t baudRate\_Bps

Desired baud rate in bits per second.

bool enableTimeout

Enable internal timeout function.

```
struct _i2c_master_transfer
```

#include <fsl\_i2c.h> Non-blocking transfer descriptor structure.

This structure is used to pass transaction parameters to the I2C\_MasterTransferNonBlocking() API.

### **Public Members**

uint32\_t flags

Bit mask of options for the transfer. See enumeration \_i2c\_master\_transfer\_flags for available options. Set to 0 or kI2C\_TransferDefaultFlag for normal transfers.

 $uint16_t$  slaveAddress

The 7-bit slave address.

 $i2c\_direction\_t$  direction

Either kI2C\_Read or kI2C\_Write.

 $uint32\_t \; \mathrm{subaddress}$ 

Sub address. Transferred MSB first.

 $size_t subaddressSize$ 

Length of sub address to send in bytes. Maximum size is 4 bytes.

void \*data

Pointer to data to transfer.

 $size\_t dataSize$ 

Number of bytes to transfer.

 $struct _i2c_master_handle$ 

#include <fsl\_i2c.h> Driver handle for master non-blocking APIs.

**Note:** The contents of this structure are private and subject to change.

### **Public Members**

 $uint8\_t state$ 

Transfer state machine current state.

uint32\_t transferCount

Indicates progress of the transfer

uint32 t remainingBytes

Remaining byte count in current state.

uint8 t\*buf

Buffer pointer for current state.

*i2c\_master\_transfer\_t* transfer

Copy of the current transfer info.

*i2c\_master\_transfer\_callback\_t* completionCallback

Callback function pointer.

void \*userData

Application data passed to callback.

# 2.7 I2C Slave Driver

void I2C SlaveGetDefaultConfig(i2c\_slave\_config\_t \*slaveConfig)

Provides a default configuration for the I2C slave peripheral.

This function provides the following default configuration for the I2C slave peripheral:

```
slaveConfig->enableSlave = true;
slaveConfig->address0.disable = false;
slaveConfig->address0.address = 0u;
slaveConfig->address1.disable = true;
slaveConfig->address2.disable = true;
slaveConfig->address3.disable = true;
slaveConfig->busSpeed = kI2C_SlaveStandardMode;
```

After calling this function, override any settings to customize the configuration, prior to initializing the master driver with I2C\_SlaveInit(). Be sure to override at least the *address0.address* member of the configuration structure with the desired slave address.

#### **Parameters**

• slaveConfig – **[out]** User provided configuration structure that is set to default values. Refer to i2c slave config t.

```
status_t I2C_SlaveInit(I2C_Type *base, const i2c_slave_config_t *slaveConfig, uint32_t srcClock_Hz)
```

Initializes the I2C slave peripheral.

This function enables the peripheral clock and initializes the I2C slave peripheral as described by the user provided configuration.

### **Parameters**

- base The I2C peripheral base address.
- slaveConfig User provided peripheral configuration. Use I2C\_SlaveGetDefaultConfig() to get a set of defaults that you can override.
- srcClock\_Hz Frequency in Hertz of the I2C functional clock. Used to calculate CLKDIV value to provide enough data setup time for master when slave stretches the clock.

void I2C\_SlaveSetAddress(I2C\_Type \*base, *i2c\_slave\_address\_register\_t* addressRegister, uint8\_t address, bool addressDisable)

Configures Slave Address n register.

This function writes new value to Slave Address register.

#### **Parameters**

- base The I2C peripheral base address.
- addressRegister The module supports multiple address registers. The parameter determines which one shall be changed.
- address The slave address to be stored to the address register for matching.
- addressDisable Disable matching of the specified address register.

void I2C\_SlaveDeinit(I2C\_Type \*base)

Deinitializes the I2C slave peripheral.

This function disables the I2C slave peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

### **Parameters**

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• base – The I2C peripheral base address.

static inline void I2C SlaveEnable(I2C\_Type \*base, bool enable)

Enables or disables the I2C module as slave.

### **Parameters**

- base The I2C peripheral base address.
- enable True to enable or flase to disable.

static inline void I2C\_SlaveClearStatusFlags(I2C\_Type \*base, uint32\_t statusMask)

Clears the I2C status flag state.

The following status register flags can be cleared:

· slave deselected flag

Attempts to clear other flags has no effect.

### See also:

\_i2c\_slave\_flags.

### **Parameters**

- base The I2C peripheral base address.
- statusMask A bitmask of status flags that are to be cleared. The mask is composed of \_i2c\_slave\_flags enumerators OR'd together. You may pass the result of a previous call to I2C\_SlaveGetStatusFlags().

 $status\_t \ {\tt I2C\_SlaveWriteBlocking}(I2C\_Type \ *base, const \ uint8\_t \ *txBuff, size\_t \ txSize)$ 

Performs a polling send transfer on the I2C bus.

The function executes blocking address phase and blocking data phase.

### **Parameters**

- base The I2C peripheral base address.
- txBuff The pointer to the data to be transferred.
- txSize The length in bytes of the data to be transferred.

#### **Returns**

kStatus\_Success Data has been sent.

### **Returns**

kStatus\_Fail Unexpected slave state (master data write while master read from slave is expected).

status\_t I2C\_SlaveReadBlocking(I2C\_Type \*base, uint8\_t \*rxBuff, size\_t rxSize)

Performs a polling receive transfer on the I2C bus.

The function executes blocking address phase and blocking data phase.

#### **Parameters**

- base The I2C peripheral base address.
- rxBuff The pointer to the data to be transferred.
- rxSize The length in bytes of the data to be transferred.

#### **Returns**

kStatus\_Success Data has been received.

### **Returns**

kStatus\_Fail Unexpected slave state (master data read while master write to slave is expected).

 $\label{local_solution} \begin{tabular}{ll} void I2C\_SlaveTransferCreateHandle(I2C\_Type *base, $i2c\_slave\_handle\_t$ *handle, \\ $i2c\_slave\_transfer\_callback\_t$ callback, void *userData) \\ \end{tabular}$ 

Creates a new handle for the I2C slave non-blocking APIs.

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the I2C SlaveTransferAbort() API shall be called.

#### **Parameters**

- $\bullet \ {\rm base}$  The I2C peripheral base address.
- handle **[out]** Pointer to the I2C slave driver handle.
- callback User provided pointer to the asynchronous callback function.
- userData User provided pointer to the application callback data.

Starts accepting slave transfers.

Call this API after calling I2C\_SlaveInit() and I2C\_SlaveTransferCreateHandle() to start processing transactions driven by an I2C master. The slave monitors the I2C bus and pass events to the callback that was passed into the call to I2C\_SlaveTransferCreateHandle(). The callback is always invoked from the interrupt context.

If no slave Tx transfer is busy, a master read from slave request invokes kI2C\_SlaveTransmitEvent callback. If no slave Rx transfer is busy, a master write to slave request invokes kI2C\_SlaveReceiveEvent callback.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of i2c\_slave\_transfer\_event\_t enumerators for the events you wish to receive. The kI2C\_SlaveTransmitEvent and kI2C\_SlaveReceiveEvent events are always enabled and do not need to be included in the mask. Alternatively, you can pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the kI2C\_SlaveAllEvents constant is provided as a convenient way to enable all events.

### **Parameters**

- base The I2C peripheral base address.
- handle Pointer to i2c\_slave\_handle\_t structure which stores the transfer state.
- eventMask Bit mask formed by OR'ing together i2c\_slave\_transfer\_event\_t enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and kI2C SlaveAllEvents to enable all events.

#### **Return values**

- kStatus\_Success Slave transfers were successfully started.
- $\bullet~{\rm kStatus\_I2C\_Busy}$  Slave transfers have already been started on this handle.

status\_t I2C\_SlaveSetSendBuffer(I2C\_Type \*base, volatile i2c\_slave\_transfer\_t \*transfer, const void \*txData, size\_t txSize, uint32\_t eventMask)

Starts accepting master read from slave requests.

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The function can be called in response to kI2C\_SlaveTransmitEvent callback to start a new slave Tx transfer from within the transfer callback.

The set of events received by the callback is customizable. To do so, set the <code>eventMask</code> parameter to the OR'd combination of i2c\_slave\_transfer\_event\_t enumerators for the events you wish to receive. The kI2C\_SlaveTransmitEvent and kI2C\_SlaveReceiveEvent events are always enabled and do not need to be included in the mask. Alternatively, you can pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the kI2C\_SlaveAllEvents constant is provided as a convenient way to enable all events.

#### **Parameters**

- base The I2C peripheral base address.
- transfer Pointer to i2c\_slave\_transfer\_t structure.
- txData Pointer to data to send to master.
- txSize Size of txData in bytes.
- eventMask Bit mask formed by OR'ing together i2c\_slave\_transfer\_event\_t enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and kI2C\_SlaveAllEvents to enable all events.

#### Return values

- kStatus\_Success Slave transfers were successfully started.
- $kStatus\_I2C\_Busy$  Slave transfers have already been started on this handle.

status\_t I2C\_SlaveSetReceiveBuffer(I2C\_Type \*base, volatile i2c\_slave\_transfer\_t \*transfer, void \*rxData, size\_t rxSize, uint32\_t eventMask)

Starts accepting master write to slave requests.

The function can be called in response to kI2C\_SlaveReceiveEvent callback to start a new slave Rx transfer from within the transfer callback.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of i2c\_slave\_transfer\_event\_t enumerators for the events you wish to receive. The kI2C\_SlaveTransmitEvent and kI2C\_SlaveReceiveEvent events are always enabled and do not need to be included in the mask. Alternatively, you can pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the kI2C\_SlaveAllEvents constant is provided as a convenient way to enable all events.

#### **Parameters**

- base The I2C peripheral base address.
- transfer Pointer to i2c slave transfer t structure.
- rxData Pointer to data to store data from master.
- rxSize Size of rxData in bytes.
- eventMask Bit mask formed by OR'ing together i2c\_slave\_transfer\_event\_t enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and kI2C\_SlaveAllEvents to enable all events.

# **Return values**

- kStatus Success Slave transfers were successfully started.
- kStatus\_I2C\_Busy Slave transfers have already been started on this handle.

static inline uint 32\_t I2C\_SlaveGetReceivedAddress(I2C\_Type \*base, volatile  $i2c\_slave\_transfer\_t$  \*transfer)

Returns the slave address sent by the I2C master.

This function should only be called from the address match event callback kI2C\_SlaveAddressMatchEvent.

#### **Parameters**

- base The I2C peripheral base address.
- transfer The I2C slave transfer.

#### Returns

The 8-bit address matched by the I2C slave. Bit 0 contains the R/w direction bit, and the 7-bit slave address is in the upper 7 bits.

void I2C\_SlaveTransferAbort(I2C\_Type \*base, i2c\_slave\_handle\_t \*handle)
Aborts the slave non-blocking transfers.

**Note:** This API could be called at any time to stop slave for handling the bus events.

### **Parameters**

- base The I2C peripheral base address.
- handle Pointer to i2c\_slave\_handle\_t structure which stores the transfer state.

### **Return values**

- kStatus Success -
- kStatus I2C Idle –

status\_t I2C\_SlaveTransferGetCount(I2C\_Type \*base, i2c\_slave\_handle\_t \*handle, size\_t \*count)

Gets the slave transfer remaining bytes during a interrupt non-blocking transfer.

### **Parameters**

- base I2C base pointer.
- handle pointer to i2c\_slave\_handle\_t structure.
- count Number of bytes transferred so far by the non-blocking transaction.

### **Return values**

- kStatus\_InvalidArgument count is Invalid.
- $kStatus\_Success$  Successfully return the count.

void I2C SlaveTransferHandleIRQ(I2C\_Type \*base, void \*i2cHandle)

Reusable routine to handle slave interrupts.

**Note:** This function does not need to be called unless you are reimplementing the non blocking API's interrupt handler routines to add special functionality.

#### **Parameters**

- base The I2C peripheral base address.
- i2cHandle Pointer to  $i2c\_slave\_handle\_t$  structure which stores the transfer state.

2.7. I2C Slave Driver

```
enum _i2c_slave_flags
     I2C slave peripheral flags.
     Note: These enums are meant to be OR'd together to form a bit mask.
     Values:
     enumerator kI2C SlavePendingFlag
         The I2C module is waiting for software interaction.
     enumerator kI2C SlaveNotStretching
         Indicates whether the slave is currently stretching clock (0 = yes, 1 = no).
     enumerator kI2C SlaveSelected
         Indicates whether the slave is selected by an address match.
     enumerator kI2C SaveDeselected
         Indicates that slave was previously deselected (deselect event took place, w1c).
enum i2c slave address register
     I2C slave address register.
     Values:
     enumerator kI2C_SlaveAddressRegister0
         Slave Address 0 register.
     enumerator kI2C_SlaveAddressRegister1
         Slave Address 1 register.
     enumerator kI2C_SlaveAddressRegister2
         Slave Address 2 register.
     enumerator kI2C SlaveAddressRegister3
         Slave Address 3 register.
enum _i2c_slave_address_qual_mode
     I2C slave address match options.
     Values:
     enumerator kI2C QualModeMask
         The SLVQUALO field (qualAddress) is used as a logical mask for matching address0.
     enumerator kI2C_QualModeExtend
         The SLVQUAL0 (qualAddress) field is used to extend address 0 matching in a range of
         addresses.
enum _i2c_slave_bus_speed
     I2C slave bus speed options.
     Values:
     enumerator kI2C SlaveStandardMode
     enumerator kI2C SlaveFastMode
     enumerator kI2C SlaveFastModePlus
     enumerator kI2C_SlaveHsMode
```

```
enum i2c slave transfer event
```

Set of events sent to the callback for non blocking slave transfers.

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to I2C\_SlaveTransferNonBlocking() in order to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

**Note:** These enumerations are meant to be OR'd together to form a bit mask of events.

```
Values:
```

enumerator kI2C SlaveAddressMatchEvent

Received the slave address after a start or repeated start.

enumerator kI2C SlaveTransmitEvent

Callback is requested to provide data to transmit (slave-transmitter role).

enumerator kI2C SlaveReceiveEvent

Callback is requested to provide a buffer in which to place received data (slave-receiver role).

enumerator kI2C SlaveCompletionEvent

All data in the active transfer have been consumed.

enumerator kI2C SlaveDeselectedEvent

The slave function has become deselected (SLVSEL flag changing from 1 to 0.

enumerator kI2C SlaveAllEvents

Bit mask of all available events.

```
enum i2c slave fsm
```

I2C slave software finite state machine states.

Values:

enumerator kI2C SlaveFsmAddressMatch

enumerator kI2C\_SlaveFsmReceive

enumerator kI2C SlaveFsmTransmit

 $typedef\ enum\_i2c\_slave\_address\_register\ i2c\_slave\_address\_register\_t$ 

I2C slave address register.

typedef struct i2c slave address i2c slave address t

Data structure with 7-bit Slave address and Slave address disable.

typedef enum \_i2c\_slave\_address\_qual\_mode i2c\_slave\_address\_qual\_mode\_t

I2C slave address match options.

typedef enum \_i2c\_slave\_bus\_speed i2c\_slave\_bus\_speed\_t

I2C slave bus speed options.

 $typedef\ struct\_i2c\_slave\_config\ i2c\_slave\_config\_t$ 

Structure with settings to initialize the I2C slave module.

This structure holds configuration settings for the I2C slave peripheral. To initialize this structure to reasonable defaults, call the I2C\_SlaveGetDefaultConfig() function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

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```
typedef enum_i2c_slave_transfer_event i2c_slave_transfer_event t
```

Set of events sent to the callback for non blocking slave transfers.

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to I2C\_SlaveTransferNonBlocking() in order to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

**Note:** These enumerations are meant to be OR'd together to form a bit mask of events.

```
typedef struct _i2c_slave_handle i2c_slave_handle_t
```

I2C slave handle typedef.

```
typedef\ struct\_i2c\_slave\_transfer\ i2c\_slave\_transfer\_t
```

I2C slave transfer structure.

typedef void (\*i2c\_slave\_transfer\_callback\_t)(I2C\_Type \*base, volatile *i2c\_slave\_transfer\_t* \*transfer, void \*userData)

Slave event callback function pointer type.

This callback is used only for the slave non-blocking transfer API. To install a callback, use the I2C\_SlaveSetCallback() function after you have created a handle.

#### Param base

Base address for the I2C instance on which the event occurred.

### Param transfer

Pointer to transfer descriptor containing values passed to and/or from the callback.

# Param userData

Arbitrary pointer-sized value passed from the application.

```
typedef enum _i2c_slave_fsm i2c_slave_fsm_t
```

I2C slave software finite state machine states.

```
typedef void (*i2c_isr_t)(I2C_Type *base, void *i2cHandle)
```

Typedef for interrupt handler.

```
struct _i2c _slave _address
```

#include <fsl\_i2c.h> Data structure with 7-bit Slave address and Slave address disable.

### **Public Members**

```
uint8 t address
```

7-bit Slave address SLVADR.

bool addressDisable

Slave address disable SADISABLE.

```
struct i2c slave config
```

#include <fsl\_i2c.h> Structure with settings to initialize the I2C slave module.

This structure holds configuration settings for the I2C slave peripheral. To initialize this structure to reasonable defaults, call the I2C\_SlaveGetDefaultConfig() function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

### **Public Members**

i2c slave address t address0

Slave's 7-bit address and disable.

i2c slave address t address1

Alternate slave 7-bit address and disable.

 $i2c\_slave\_address\_t$  address2

Alternate slave 7-bit address and disable.

 $i2c\_slave\_address\_t \text{ address}3$ 

Alternate slave 7-bit address and disable.

 $i2c\_slave\_address\_qual\_mode\_t$  qualMode

Qualify mode for slave address 0.

uint8\_t qualAddress

Slave address qualifier for address 0.

 $i2c\_slave\_bus\_speed\_t$  busSpeed

Slave bus speed mode. If the slave function stretches SCL to allow for software response, it must provide sufficient data setup time to the master before releasing the stretched clock. This is accomplished by inserting one clock time of CLKDIV at that point. The busSpeed value is used to configure CLKDIV such that one clock time is greater than the tSU;DAT value noted in the I2C bus specification for the I2C mode that is being used. If the busSpeed mode is unknown at compile time, use the longest data setup time kI2C\_SlaveStandardMode (250 ns)

bool enableSlave

Enable slave mode.

struct \_i2c\_slave\_transfer

#include <fsl\_i2c.h> I2C slave transfer structure.

### **Public Members**

i2c slave handle t\*handle

Pointer to handle that contains this transfer.

i2c slave transfer event t event

Reason the callback is being invoked.

uint8 t receivedAddress

Matching address send by master. 7-bits plus R/nW bit0

uint32 t eventMask

Mask of enabled events.

uint8 t\*rxData

Transfer buffer for receive data

const uint8 t\*txData

Transfer buffer for transmit data

size t txSize

Transfer size

size trxSize

Transfer size

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size\_t transferredCount

Number of bytes transferred during this transfer.

status\_t completionStatus

Success or error code describing how the transfer completed. Only applies for kI2C\_SlaveCompletionEvent.

 $struct _i2c _slave _handle$ 

#include <fsl\_i2c.h> I2C slave handle structure.

**Note:** The contents of this structure are private and subject to change.

#### **Public Members**

volatile  $i2c\_slave\_transfer\_t$  transfer

I2C slave transfer.

volatile bool isBusy

Whether transfer is busy.

volatile *i2c\_slave\_fsm\_t* slaveFsm

slave transfer state machine.

*i2c\_slave\_transfer\_callback\_t* callback

Callback function called at transfer event.

void \*userData

Callback parameter passed to callback.

# 2.8 IAP: In Application Programming Driver

status t IAP ReadPartID(uint32 t \*partID)

Read part identification number.

This function is used to read the part identification number.

# **Parameters**

• partID – Address to store the part identification number.

# **Return values**

kStatus IAP Success – Api has been executed successfully.

status\_t IAP\_ReadBootCodeVersion(uint32\_t \*bootCodeVersion)

Read boot code version number.

This function is used to read the boot code version number.

note Boot code version is two 32-bit words. Word 0 is the major version, word 1 is the minor version.

### **Parameters**

• bootCodeVersion – Address to store the boot code version.

### **Return values**

kStatus\_IAP\_Success – Api has been executed successfully.

void IAP ReinvokeISP(uint8\_t ispType, uint32\_t \*status)

Reinvoke ISP.

This function is used to invoke the boot loader in ISP mode. It maps boot vectors and configures the peripherals for ISP.

note The error response will be returned when IAP is disabled or an invalid ISP type selection appears. The call won't return unless an error occurs, so there can be no status code.

#### **Parameters**

- ispType ISP type selection.
- status store the possible status.

### **Return values**

kStatus\_IAP\_ReinvokeISPConfig - reinvoke configuration error.

 $status\_t \text{ IAP}\_\text{ReadUniqueID}(uint32\_t *uniqueID)$ 

Read unique identification.

This function is used to read the unique id.

#### **Parameters**

• uniqueID – store the uniqueID.

# **Return values**

kStatus\_IAP\_Success - Api has been executed successfully.

status\_t IAP\_PrepareSectorForWrite(uint32\_t startSector, uint32\_t endSector)

Prepare sector for write operation.

This function prepares sector(s) for write/erase operation. This function must be called before calling the IAP\_CopyRamToFlash() or IAP\_EraseSector() or IAP\_ErasePage() function. The end sector number must be greater than or equal to the start sector number.

### **Parameters**

- startSector Start sector number.
- endSector End sector number.

### **Return values**

- kStatus\_IAP\_Success Api has been executed successfully.
- kStatus\_IAP\_NoPower Flash memory block is powered down.
- kStatus IAP NoClock Flash memory block or controller is not clocked.
- kStatus\_IAP\_InvalidSector Sector number is invalid or end sector number is greater than start sector number.
- kStatus IAP Busy Flash programming hardware interface is busy.

Copy RAM to flash.

This function programs the flash memory. Corresponding sectors must be prepared via IAP\_PrepareSectorForWrite before calling this function.

#### **Parameters**

 dstAddr – Destination flash address where data bytes are to be written, the address should be multiples of FSL FEATURE SYSCON FLASH PAGE SIZE BYTES boundary.

- srcAddr Source ram address from where data bytes are to be read.
- numOfBytes Number of bytes to be written, it should be multiples of FSL\_FEATURE\_SYSCON\_FLASH\_PAGE\_SIZE\_BYTES, and ranges from FSL\_FEATURE\_SYSCON\_FLASH\_PAGE\_SIZE\_BYTES to FSL\_FEATURE\_SYSCON\_FLASH\_SECTOR\_SIZE\_BYTES.
- systemCoreClock SystemCoreClock in Hz. It is converted to KHz before calling the rom IAP function. When the flash controller has a fixed reference clock, this parameter is bypassed.

### **Return values**

- kStatus IAP Success Api has been executed successfully.
- kStatus IAP NoPower Flash memory block is powered down.
- kStatus IAP NoClock Flash memory block or controller is not clocked.
- kStatus IAP SrcAddrError Source address is not on word boundary.
- kStatus\_IAP\_DstAddrError Destination address is not on a correct boundary.
- kStatus\_IAP\_SrcAddrNotMapped Source address is not mapped in the memory map.
- kStatus\_IAP\_DstAddrNotMapped Destination address is not mapped in the memory map.
- kStatus\_IAP\_CountError Byte count is not multiple of 4 or is not a permitted value.
- kStatus\_IAP\_NotPrepared Command to prepare sector for write operation has not been executed.
- kStatus\_IAP\_Busy Flash programming hardware interface is busy.

This function erases sector(s). The end sector number must be greater than or equal to the start sector number.

### **Parameters**

- startSector Start sector number.
- endSector End sector number.
- systemCoreClock SystemCoreClock in Hz. It is converted to KHz before calling the rom IAP function. When the flash controller has a fixed reference clock, this parameter is bypassed.

# **Return values**

- kStatus IAP Success Api has been executed successfully.
- kStatus\_IAP\_NoPower Flash memory block is powered down.
- kStatus\_IAP\_NoClock Flash memory block or controller is not clocked.
- kStatus\_IAP\_InvalidSector Sector number is invalid or end sector number is greater than start sector number.
- kStatus\_IAP\_NotPrepared Command to prepare sector for write operation has not been executed.
- kStatus\_IAP\_Busy Flash programming hardware interface is busy.

status\_t IAP\_ErasePage(uint32\_t startPage, uint32\_t endPage, uint32\_t systemCoreClock) Erase page.

This function erases page(s). The end page number must be greater than or equal to the start page number.

#### **Parameters**

- startPage Start page number.
- endPage End page number.
- systemCoreClock SystemCoreClock in Hz. It is converted to KHz before calling the rom IAP function. When the flash controller has a fixed reference clock, this parameter is bypassed.

### Return values

- kStatus\_IAP\_Success Api has been executed successfully.
- kStatus\_IAP\_NoPower Flash memory block is powered down.
- kStatus\_IAP\_NoClock Flash memory block or controller is not clocked.
- kStatus\_IAP\_InvalidSector Page number is invalid or end page number is greater than start page number.
- kStatus\_IAP\_NotPrepared Command to prepare sector for write operation has not been executed.
- kStatus\_IAP\_Busy Flash programming hardware interface is busy.

status\_t IAP\_BlankCheckSector(uint32\_t startSector, uint32\_t endSector)

Blank check sector(s)

Blank check single or multiples sectors of flash memory. The end sector number must be greater than or equal to the start sector number. It can be used to verify the sector erasure after IAP\_EraseSector call.

### **Parameters**

- startSector Start sector number.
- endSector End sector number.

### **Return values**

- kStatus IAP Success One or more sectors are in erased state.
- kStatus IAP NoPower Flash memory block is powered down.
- kStatus IAP NoClock Flash memory block or controller is not clocked.
- kStatus IAP SectorNotblank One or more sectors are not blank.

status\_t IAP\_Compare(uint32\_t dstAddr, uint32\_t \*srcAddr, uint32\_t numOfBytes)

Compare memory contents of flash with ram.

This function compares the contents of flash and ram. It can be used to verify the flash memory contents after IAP\_CopyRamToFlash call.

### **Parameters**

- dstAddr Destination flash address.
- srcAddr Source ram address.
- numOfBytes Number of bytes to be compared.

### **Return values**

• kStatus IAP Success – Contents of flash and ram match.

- kStatus IAP NoPower Flash memory block is powered down.
- kStatus IAP NoClock Flash memory block or controller is not clocked.
- kStatus\_IAP\_AddrError Address is not on word boundary.
- kStatus\_IAP\_AddrNotMapped Address is not mapped in the memory map.
- kStatus\_IAP\_CountError Byte count is not multiple of 4 or is not a permitted value.
- kStatus\_IAP\_CompareError Destination and source memory contents do not match.

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```
iap status codes.
```

Values:

enumerator kStatus\_IAP\_Success

Api is executed successfully

enumerator kStatus\_IAP\_InvalidCommand

Invalid command

enumerator kStatus\_IAP\_SrcAddrError

Source address is not on word boundary

 ${\bf enumerator} \ {\rm kStatus\_IAP\_DstAddrError}$ 

Destination address is not on a correct boundary

enumerator kStatus\_IAP\_SrcAddrNotMapped

Source address is not mapped in the memory map

enumerator kStatus\_IAP\_DstAddrNotMapped

Destination address is not mapped in the memory map

enumerator kStatus IAP CountError

Byte count is not multiple of 4 or is not a permitted value

enumerator kStatus IAP InvalidSector

Sector/page number is invalid or end sector/page number is greater than start sector/page number

enumerator kStatus IAP SectorNotblank

One or more sectors are not blank

enumerator kStatus\_IAP\_NotPrepared

Command to prepare sector for write operation has not been executed

enumerator kStatus\_IAP\_CompareError

Destination and source memory contents do not match

enumerator kStatus\_IAP\_Busy

Flash programming hardware interface is busy

 $enumerator \ kStatus\_IAP\_ParamError$ 

Insufficient number of parameters or invalid parameter

enumerator kStatus\_IAP\_AddrError

Address is not on word boundary

```
enumerator kStatus_IAP_AddrNotMapped
Address is not mapped in the memory map
enumerator kStatus_IAP_NoPower
Flash memory block is powered down
enumerator kStatus_IAP_NoClock
Flash memory block or controller is not clocked
enumerator kStatus_IAP_ReinvokeISPConfig
Reinvoke configuration error
enum_iap_commands
iap command codes.

Values:
enumerator kIapCmd_IAP_ReadFactorySettings
Read the factory settings
enumerator kIapCmd_IAP_PrepareSectorforWrite
Prepare Sector for write
```

Copy RAM to flash

enumerator kIapCmd\_IAP\_BlankCheckSector Blank check sector

enumerator kIapCmd\_IAP\_CopyRamToFlash

 $\begin{array}{c} \textbf{enumerator} \; \mathrm{kIapCmd\_IAP\_ReadPartId} \\ \textbf{Read} \; \textbf{part} \; \textbf{id} \end{array}$ 

 $\begin{array}{c} \textbf{enumerator} \; \text{kIapCmd\_IAP\_Read\_BootromVersion} \\ \textbf{Read bootrom version} \end{array}$ 

 $\begin{array}{c} \textbf{enumerator} \; \text{kIapCmd\_IAP\_Compare} \\ \textbf{Compare} \end{array}$ 

enumerator  $kIapCmd\_IAP\_ReinvokeISP$ Reinvoke ISP

 $\begin{array}{c} \textbf{enumerator} \; \text{kIapCmd\_IAP\_ReadUid} \\ \textbf{Read} \; \textbf{Uid} \end{array}$ 

 $\begin{array}{c} \textbf{enumerator} \; \text{kIapCmd\_IAP\_ErasePage} \\ \textbf{Erase Page} \end{array}$ 

 $\begin{array}{c} \textbf{enumerator} \; \text{kIapCmd\_IAP\_ReadSignature} \\ \textbf{Read Signature} \end{array}$ 

 ${\bf enumerator} \ {\rm kIapCmd\_IAP\_ExtendedReadSignature} \\ {\bf Extended} \ {\bf Read} \ {\bf Signature} \\$ 

 $\begin{array}{c} \textbf{enumerator} \; \text{kIapCmd\_IAP\_ReadEEPROMPage} \\ \textbf{Read} \; \textbf{EEPROM} \; \textbf{page} \end{array}$ 

 $\label{eq:cmd_IAP_WriteEEPROMPage} \begin{tabular}{ll} \bf Write\,EEPROM\,page \\ \bf Write\,EEPROM\,page \\ \end{tabular}$ 

```
enum _flash_access_time
Flash memory access time.

Values:
enumerator kFlash_IAP_OneSystemClockTime
enumerator kFlash_IAP_TwoSystemClockTime
1 system clock flash access time
enumerator kFlash_IAP_ThreeSystemClockTime
```

2 system clock flash access time

# 2.9 Common Driver

- FSL\_COMMON\_DRIVER\_VERSION common driver version.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_NONE No debug console.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_UART Debug console based on UART.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_LPUART Debug console based on LPUART.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_LPSCI Debug console based on LPSCI.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_USBCDC Debug console based on USBCDC.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_FLEXCOMM Debug console based on FLEXCOMM.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_IUART Debug console based on i.MX UART.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_VUSART Debug console based on LPC\_VUSART.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_MINI\_USART Debug console based on LPC\_USART.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_SWO Debug console based on SWO.
- DEBUG\_CONSOLE\_DEVICE\_TYPE\_QSCI Debug console based on QSCI.
- MIN(a, b) Computes the minimum of a and b.
- MAX(a, b)
  - Computes the maximum of a and b.
- UINT16\_MAX

  Max value of uint16\_t type.

UINT32 MAX

Max value of uint32\_t type.

SDK ATOMIC LOCAL ADD(addr, val)

Add value val from the variable at address address.

SDK\_ATOMIC\_LOCAL\_SUB(addr, val)

Subtract value val to the variable at address address.

SDK ATOMIC LOCAL SET(addr, bits)

Set the bits specifiled by bits to the variable at address address.

SDK ATOMIC LOCAL CLEAR(addr, bits)

Clear the bits specifiled by bits to the variable at address address.

SDK\_ATOMIC\_LOCAL\_TOGGLE(addr, bits)

Toggle the bits specifiled by bits to the variable at address address.

SDK\_ATOMIC\_LOCAL\_CLEAR\_AND\_SET(addr, clearBits, setBits)

For the variable at address *address*, clear the bits specifiled by *clearBits* and set the bits specifiled by *setBits*.

SDK\_ATOMIC\_LOCAL\_COMPARE\_AND\_SET(addr, expected, newValue)

For the variable at address *address*, check whether the value equal to *expected*. If value same as *expected* then update *newValue* to address and return **true**, else return **false**.

SDK\_ATOMIC\_LOCAL\_TEST\_AND\_SET(addr, newValue)

For the variable at address address, set as newValue value and return old value.

USEC TO COUNT(us, clockFreqInHz)

Macro to convert a microsecond period to raw count value

COUNT\_TO\_USEC(count, clockFreqInHz)

Macro to convert a raw count value to microsecond

MSEC TO COUNT(ms, clockFreqInHz)

Macro to convert a millisecond period to raw count value

COUNT TO MSEC(count, clockFreqInHz)

Macro to convert a raw count value to millisecond

SDK ISR EXIT BARRIER

SDK\_SIZEALIGN(var, alignbytes)

Macro to define a variable with L1 d-cache line size alignment

Macro to define a variable with L2 cache line size alignment

Macro to change a value to a given size aligned value

AT NONCACHEABLE SECTION(var)

Define a variable var, and place it in non-cacheable section.

AT NONCACHEABLE SECTION ALIGN(var, alignbytes)

Define a variable *var*, and place it in non-cacheable section, the start address of the variable is aligned to *alignbytes*.

AT NONCACHEABLE SECTION INIT(var)

Define a variable *var* with initial value, and place it in non-cacheable section.

AT NONCACHEABLE\_SECTION\_ALIGN\_INIT(var, alignbytes)

Define a variable *var* with initial value, and place it in non-cacheable section, the start address of the variable is aligned to *alignbytes*.

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```
enum _status_groups
```

Status group numbers.

Values:

enumerator kStatusGroup\_Generic

Group number for generic status codes.

enumerator kStatusGroup FLASH

Group number for FLASH status codes.

enumerator kStatusGroup\_LPSPI

Group number for LPSPI status codes.

enumerator kStatusGroup FLEXIO SPI

Group number for FLEXIO SPI status codes.

enumerator kStatusGroup DSPI

Group number for DSPI status codes.

enumerator kStatusGroup\_FLEXIO\_UART

Group number for FLEXIO UART status codes.

enumerator kStatusGroup\_FLEXIO\_I2C

Group number for FLEXIO I2C status codes.

 ${\bf enumerator} \ {\rm kStatusGroup\_LPI2C}$ 

Group number for LPI2C status codes.

enumerator kStatusGroup\_UART

Group number for UART status codes.

enumerator kStatusGroup\_I2C

Group number for UART status codes.

enumerator kStatusGroup LPSCI

Group number for LPSCI status codes.

enumerator kStatusGroup LPUART

Group number for LPUART status codes.

 $enumerator \ \mathrm{kStatusGroup\_SPI}$ 

Group number for SPI status code.

enumerator kStatusGroup\_XRDC

Group number for XRDC status code.

enumerator kStatusGroup SEMA42

Group number for SEMA42 status code.

enumerator kStatusGroup SDHC

Group number for SDHC status code

 ${\bf enumerator} \; {\rm kStatusGroup\_SDMMC}$ 

Group number for SDMMC status code

 $enumerator~\mathrm{kStatusGroup\_SAI}$ 

Group number for SAI status code

enumerator kStatusGroup MCG

Group number for MCG status codes.

enumerator kStatusGroup SCG

Group number for SCG status codes.

 $enumerator~{\rm kStatusGroup\_SDSPI}$ 

Group number for SDSPI status codes.

enumerator kStatusGroup\_FLEXIO\_I2S

Group number for FLEXIO I2S status codes

enumerator kStatusGroup\_FLEXIO\_MCULCD

Group number for FLEXIO LCD status codes

enumerator kStatusGroup FLASHIAP

Group number for FLASHIAP status codes

enumerator kStatusGroup\_FLEXCOMM\_I2C

Group number for FLEXCOMM I2C status codes

 $enumerator~{\rm kStatusGroup\_I2S}$ 

Group number for I2S status codes

enumerator kStatusGroup\_IUART

Group number for IUART status codes

enumerator kStatusGroup\_CSI

Group number for CSI status codes

enumerator kStatusGroup\_MIPI\_DSI

Group number for MIPI DSI status codes

enumerator kStatusGroup\_SDRAMC

Group number for SDRAMC status codes.

enumerator kStatusGroup\_POWER

Group number for POWER status codes.

enumerator kStatusGroup\_ENET

Group number for ENET status codes.

enumerator kStatusGroup\_PHY

Group number for PHY status codes.

enumerator kStatusGroup TRGMUX

Group number for TRGMUX status codes.

enumerator kStatusGroup\_SMARTCARD

Group number for SMARTCARD status codes.

enumerator kStatusGroup\_LMEM

Group number for LMEM status codes.

enumerator kStatusGroup\_QSPI

Group number for QSPI status codes.

enumerator kStatusGroup\_DMA

Group number for DMA status codes.

enumerator kStatusGroup\_EDMA

Group number for EDMA status codes.

enumerator kStatusGroup\_DMAMGR

Group number for DMAMGR status codes.

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enumerator kStatusGroup\_FLEXCAN

Group number for FlexCAN status codes.

enumerator kStatusGroup\_LTC

Group number for LTC status codes.

enumerator kStatusGroup\_FLEXIO\_CAMERA

Group number for FLEXIO CAMERA status codes.

enumerator kStatusGroup\_LPC\_SPI

Group number for LPC\_SPI status codes.

enumerator kStatusGroup LPC USART

Group number for LPC\_USART status codes.

 $enumerator~\mathrm{kStatusGroup\_DMIC}$ 

Group number for DMIC status codes.

enumerator kStatusGroup\_SDIF

Group number for SDIF status codes.

enumerator kStatusGroup\_SPIFI

Group number for SPIFI status codes.

enumerator kStatusGroup\_OTP

Group number for OTP status codes.

enumerator kStatusGroup\_MCAN

Group number for MCAN status codes.

enumerator kStatusGroup\_CAAM

Group number for CAAM status codes.

enumerator kStatusGroup\_ECSPI

Group number for ECSPI status codes.

enumerator kStatusGroup\_USDHC

Group number for USDHC status codes.

enumerator kStatusGroup\_LPC\_I2C

Group number for LPC\_I2C status codes.

enumerator kStatusGroup DCP

Group number for DCP status codes.

enumerator kStatusGroup\_MSCAN

Group number for MSCAN status codes.

enumerator kStatusGroup\_ESAI

Group number for ESAI status codes.

enumerator kStatusGroup\_FLEXSPI

Group number for FLEXSPI status codes.

enumerator kStatusGroup\_MMDC

Group number for MMDC status codes.

enumerator kStatusGroup\_PDM

Group number for MIC status codes.

enumerator kStatusGroup\_SDMA

Group number for SDMA status codes.

enumerator kStatusGroup\_ICS

Group number for ICS status codes.

enumerator kStatusGroup\_SPDIF

Group number for SPDIF status codes.

enumerator kStatusGroup\_LPC\_MINISPI

Group number for LPC\_MINISPI status codes.

enumerator kStatusGroup HASHCRYPT

Group number for Hashcrypt status codes

enumerator kStatusGroup LPC SPI SSP

Group number for LPC\_SPI\_SSP status codes.

enumerator kStatusGroup\_I3C

Group number for I3C status codes

enumerator kStatusGroup\_LPC\_I2C\_1

Group number for LPC\_I2C\_1 status codes.

enumerator kStatusGroup\_NOTIFIER

Group number for NOTIFIER status codes.

 ${\bf enumerator} \ {\rm kStatusGroup\_DebugConsole}$ 

Group number for debug console status codes.

enumerator kStatusGroup\_SEMC

Group number for SEMC status codes.

 $enumerator \ kStatusGroup\_ApplicationRangeStart$ 

Starting number for application groups.

enumerator kStatusGroup\_IAP

Group number for IAP status codes

enumerator kStatusGroup\_SFA

Group number for SFA status codes

enumerator kStatusGroup\_SPC

Group number for SPC status codes.

enumerator kStatusGroup PUF

Group number for PUF status codes.

enumerator kStatusGroup\_TOUCH\_PANEL

Group number for touch panel status codes

enumerator kStatusGroup\_VBAT

Group number for VBAT status codes

enumerator kStatusGroup\_XSPI

Group number for XSPI status codes

enumerator kStatusGroup\_PNGDEC

Group number for PNGDEC status codes

 ${\bf enumerator} \ {\rm kStatusGroup\_JPEGDEC}$ 

Group number for JPEGDEC status codes

enumerator kStatusGroup\_HAL\_GPIO

Group number for HAL GPIO status codes.

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enumerator kStatusGroup\_HAL\_UART

Group number for HAL UART status codes.

 $enumerator~\mathrm{kStatusGroup\_HAL\_TIMER}$ 

Group number for HAL TIMER status codes.

enumerator kStatusGroup\_HAL\_SPI

Group number for HAL SPI status codes.

enumerator kStatusGroup HAL I2C

Group number for HAL I2C status codes.

enumerator kStatusGroup HAL FLASH

Group number for HAL FLASH status codes.

enumerator kStatusGroup HAL PWM

Group number for HAL PWM status codes.

enumerator kStatusGroup\_HAL\_RNG

Group number for HAL RNG status codes.

enumerator kStatusGroup\_HAL\_I2S

Group number for HAL I2S status codes.

enumerator kStatusGroup\_HAL\_ADC\_SENSOR

Group number for HAL ADC SENSOR status codes.

enumerator kStatusGroup\_TIMERMANAGER

Group number for TiMER MANAGER status codes.

enumerator kStatusGroup\_SERIALMANAGER

Group number for SERIAL MANAGER status codes.

enumerator kStatusGroup\_LED

Group number for LED status codes.

enumerator kStatusGroup\_BUTTON

Group number for BUTTON status codes.

enumerator kStatusGroup\_EXTERN\_EEPROM

Group number for EXTERN EEPROM status codes.

enumerator kStatusGroup SHELL

Group number for SHELL status codes.

enumerator kStatusGroup\_MEM\_MANAGER

Group number for MEM MANAGER status codes.

enumerator kStatusGroup\_LIST

Group number for List status codes.

enumerator kStatusGroup\_OSA

Group number for OSA status codes.

enumerator kStatusGroup\_COMMON\_TASK

Group number for Common task status codes.

enumerator kStatusGroup\_MSG

Group number for messaging status codes.

enumerator kStatusGroup\_SDK\_OCOTP

Group number for OCOTP status codes.

enumerator kStatusGroup\_SDK\_FLEXSPINOR

Group number for FLEXSPINOR status codes.

enumerator kStatusGroup\_CODEC

Group number for codec status codes.

enumerator kStatusGroup\_ASRC

Group number for codec status ASRC.

enumerator kStatusGroup OTFAD

Group number for codec status codes.

enumerator kStatusGroup SDIOSLV

Group number for SDIOSLV status codes.

enumerator kStatusGroup\_MECC

Group number for MECC status codes.

 $enumerator \ kStatusGroup\_ENET\_QOS$ 

Group number for ENET\_QOS status codes.

enumerator kStatusGroup\_LOG

Group number for LOG status codes.

enumerator kStatusGroup\_I3CBUS

Group number for I3CBUS status codes.

enumerator kStatusGroup\_QSCI

Group number for QSCI status codes.

enumerator kStatusGroup\_ELEMU

Group number for ELEMU status codes.

enumerator kStatusGroup\_QUEUEDSPI

Group number for QSPI status codes.

enumerator kStatusGroup\_POWER\_MANAGER

Group number for POWER\_MANAGER status codes.

enumerator kStatusGroup\_IPED

Group number for IPED status codes.

enumerator kStatusGroup ELS PKC

Group number for ELS PKC status codes.

enumerator kStatusGroup\_CSS\_PKC

Group number for CSS PKC status codes.

enumerator kStatusGroup\_HOSTIF

Group number for HOSTIF status codes.

enumerator kStatusGroup\_CLIF

Group number for CLIF status codes.

enumerator kStatusGroup\_BMA

Group number for BMA status codes.

enumerator kStatusGroup\_NETC

Group number for NETC status codes.

enumerator kStatusGroup\_ELE

Group number for ELE status codes.

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enumerator kStatusGroup\_GLIKEY

Group number for GLIKEY status codes.

enumerator kStatusGroup\_AON\_POWER

Group number for AON\_POWER status codes.

enumerator kStatusGroup\_AON\_COMMON

Group number for AON\_COMMON status codes.

enumerator kStatusGroup\_ENDAT3

Group number for ENDAT3 status codes.

enumerator kStatusGroup HIPERFACE

Group number for HIPERFACE status codes.

enumerator kStatusGroup\_NPX

Group number for NPX status codes.

enumerator kStatusGroup\_ELA\_CSEC

Group number for ELA\_CSEC status codes.

 ${\bf enumerator}~{\rm kStatusGroup\_FLEXIO\_T\_FORMAT}$ 

Group number for T-format status codes.

 $enumerator \ kStatusGroup\_FLEXIO\_A\_FORMAT$ 

Group number for A-format status codes.

Generic status return codes.

Values:

enumerator kStatus Success

Generic status for Success.

enumerator kStatus Fail

Generic status for Fail.

enumerator kStatus ReadOnly

Generic status for read only failure.

 $enumerator~kStatus\_OutOfRange$ 

Generic status for out of range access.

enumerator kStatus\_InvalidArgument

Generic status for invalid argument check.

enumerator kStatus Timeout

Generic status for timeout.

enumerator kStatus NoTransferInProgress

Generic status for no transfer in progress.

 $enumerator~\mathrm{kStatus\_Busy}$ 

Generic status for module is busy.

 ${\bf enumerator} \; {\rm kStatus\_NoData}$ 

Generic status for no data is found for the operation.

typedef int32\_t status t

Type used for all status and error return values.

void \*SDK Malloc(size\_t size, size\_t alignbytes)

Allocate memory with given alignment and aligned size.

This is provided to support the dynamically allocated memory used in cache-able region.

#### **Parameters**

- $\operatorname{size}$  The length required to malloc.
- alignbytes The alignment size.

### **Return values**

The – allocated memory.

void SDK Free(void \*ptr)

Free memory.

### **Parameters**

• ptr – The memory to be release.

void SDK DelayAtLeastUs(uint32\_t delayTime\_us, uint32\_t coreClock\_Hz)

Delay at least for some time. Please note that, this API uses while loop for delay, different run-time environments make the time not precise, if precise delay count was needed, please implement a new delay function with hardware timer.

#### **Parameters**

- delayTime\_us Delay time in unit of microsecond.
- coreClock\_Hz Core clock frequency with Hz.

static inline status\_t EnableIRQ(IRQn\_Type interrupt)

Enable specific interrupt.

Enable LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only enables the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

# **Parameters**

• interrupt – The IRQ number.

# **Return values**

- kStatus\_Success Interrupt enabled successfully
- kStatus Fail Failed to enable the interrupt

static inline *status t* DisableIRQ(IRQn Type interrupt)

Disable specific interrupt.

Disable LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only disables the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL\_FEATURE\_NUMBER\_OF\_LEVEL1\_INT\_VECTORS.

## **Parameters**

• interrupt – The IRQ number.

### **Return values**

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- kStatus Success Interrupt disabled successfully
- kStatus Fail Failed to disable the interrupt

static inline *status\_t* EnableIRQWithPriority(IRQn\_Type interrupt, uint8\_t priNum)

Enable the IRQ, and also set the interrupt priority.

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL\_FEATURE\_NUMBER\_OF\_LEVEL1\_INT\_VECTORS.

#### **Parameters**

- interrupt The IRQ to Enable.
- priNum Priority number set to interrupt controller register.

### **Return values**

- kStatus\_Success Interrupt priority set successfully
- kStatus\_Fail Failed to set the interrupt priority.

static inline *status\_t* IRQ\_SetPriority(IRQn\_Type interrupt, uint8\_t priNum)

Set the IRQ priority.

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL\_FEATURE\_NUMBER\_OF\_LEVEL1\_INT\_VECTORS.

### **Parameters**

- interrupt The IRQ to set.
- priNum Priority number set to interrupt controller register.

# **Return values**

- kStatus Success Interrupt priority set successfully
- kStatus\_Fail Failed to set the interrupt priority.

static inline *status\_t* IRQ\_ClearPendingIRQ(IRQn\_Type interrupt)

Clear the pending IRQ flag.

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL\_FEATURE\_NUMBER\_OF\_LEVEL1\_INT\_VECTORS.

# **Parameters**

• interrupt – The flag which IRQ to clear.

## **Return values**

- kStatus Success Interrupt priority set successfully
- kStatus\_Fail Failed to set the interrupt priority.

static inline uint32\_t DisableGlobalIRQ(void)

Disable the global IRQ.

Disable the global interrupt and return the current primask register. User is required to provided the primask register for the EnableGlobalIRQ().

#### Returns

Current primask value.

static inline void EnableGlobalIRQ(uint32\_t primask)

Enable the global IRQ.

Set the primask register with the provided primask value but not just enable the primask. The idea is for the convenience of integration of RTOS. some RTOS get its own management mechanism of primask. User is required to use the EnableGlobalIRQ() and DisableGlobalIRQ() in pair.

# **Parameters**

• primask – value of primask register to be restored. The primask value is supposed to be provided by the DisableGlobalIRQ().

 $void \ {\rm Enable Deep Sleep IRQ}(IRQn\_Type \ interrupt)$ 

Enable specific interrupt for wake-up from deep-sleep mode.

Enable the interrupt for wake-up from deep sleep mode. Some interrupts are typically used in sleep mode only and will not occur during deep-sleep mode because relevant clocks are stopped. However, it is possible to enable those clocks (significantly increasing power consumption in the reduced power mode), making these wake-ups possible.

Note: This function also enables the interrupt in the NVIC (EnableIRQ() is called internaly).

# **Parameters**

• interrupt – The IRQ number.

 $void\ \mathrm{DisableDeepSleepIRQ}(IRQn\_Type\ interrupt)$ 

Disable specific interrupt for wake-up from deep-sleep mode.

Disable the interrupt for wake-up from deep sleep mode. Some interrupts are typically used in sleep mode only and will not occur during deep-sleep mode because relevant clocks are stopped. However, it is possible to enable those clocks (significantly increasing power consumption in the reduced power mode), making these wake-ups possible.

**Note:** This function also disables the interrupt in the NVIC (DisableIRQ() is called internaly).

# **Parameters**

• interrupt – The IRQ number.

 $static\ in line\ bool\ \_SDK\_AtomicLocalCompareAndSet(uint 32\_t\ * addr,\ uint 32\_t\ expected,\ uint 32\_t\ newValue)$ 

static inline uint32\_t SDK AtomicTestAndSet(uint32\_t \*addr, uint32\_t newValue)

FSL DRIVER TRANSFER DOUBLE WEAK IRQ

Macro to use the default weak IRQ handler in drivers.

MAKE STATUS(group, code)

Construct a status code value from a group and code number.

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MAKE\_VERSION(major, minor, bugfix)

Construct the version number for drivers.

The driver version is a 32-bit number, for both 32-bit platforms(such as Cortex M) and 16-bit platforms(such as DSC).

 $ARRAY_SIZE(x)$ 

Computes the number of elements in an array.

 $UINT64_H(X)$ 

Macro to get upper 32 bits of a 64-bit value

UINT64 L(X)

Macro to get lower 32 bits of a 64-bit value

SUPPRESS\_FALL\_THROUGH\_WARNING()

For switch case code block, if case section ends without "break;" statement, there wil be fallthrough warning with compiler flag -Wextra or -Wimplicit-fallthrough=n when using armgcc. To suppress this warning, "SUPPRESS\_FALL\_THROUGH\_WARNING();" need to be added at the end of each case section which misses "break;" statement.

MSDK REG SECURE ADDR(x)

Convert the register address to the one used in secure mode.

MSDK\_REG\_NONSECURE\_ADDR(x)

Convert the register address to the one used in non-secure mode.

MSDK INVALID IRQ HANDLER

Invalid IRQ handler address.

# 2.10 LPC\_ACOMP: Analog comparator Driver

void ACOMP\_Init(ACOMP\_Type \*base, const *acomp\_config\_t* \*config)
Initialize the ACOMP module.

# **Parameters**

- base ACOMP peripheral base address.
- config Pointer to "acomp\_config\_t" structure.

void ACOMP Deinit(ACOMP Type \*base)

De-initialize the ACOMP module.

# **Parameters**

• base – ACOMP peripheral base address.

void ACOMP GetDefaultConfig(acomp\_config\_t \*config)

Gets an available pre-defined settings for the ACOMP's configuration.

This function initializes the converter configuration structure with available settings. The default values are:

```
config->enableSyncToBusClk = false;
config->hysteresisSelection = kACOMP_hysteresisNoneSelection;
```

In default configuration, the ACOMP's output would be used directly and switch as the voltages cross.

#### **Parameters**

• config – Pointer to the configuration structure.

 $\label{local_comp_total} \begin{tabular}{ll} void $ACOMP\_EnableInterrupts (ACOMP\_Type *base, $acomp\_interrupt\_enable\_t$ enable) \\ Enable $ACOMP$ interrupts. \end{tabular}$ 

### **Parameters**

- base ACOMP peripheral base address.
- enable Enable/Disable interrupt feature.

 $static\ in line\ bool\ {\rm ACOMP\_GetInterruptsStatusFlags} (ACOMP\_Type\ *base)$  Get interrupts status\ flags.

### **Parameters**

• base – ACOMP peripheral base address.

#### **Returns**

Reflect the state ACOMP edge-detect status, true or false.

 $static\ in line\ void\ ACOMP\_Clear Interrupts Status Flags (ACOMP\_Type\ *base)\\ Clear\ the\ ACOMP\ interrupts\ status\ flags.$ 

#### **Parameters**

• base – ACOMP peripheral base address.

 $static\ in line\ bool\ {\rm ACOMP\_GetOutputStatusFlags} (ACOMP\_Type\ *base)$  Get ACOMP output status flags.

### **Parameters**

• base – ACOMP peripheral base address.

# Returns

Reflect the state of the comparator output, true or false.

static inline void ACOMP\_SetInputChannel(ACOMP\_Type \*base, uint32\_t postiveInputChannel, uint32\_t negativeInputChannel)

Set the ACOMP postive and negative input channel.

# **Parameters**

- base ACOMP peripheral base address.
- postiveInputChannel The index of postive input channel.
- negativeInputChannel The index of negative input channel.

 $\label{lem:config} $\operatorname{ACOMP\_SetLadderConfig}(ACOMP\_Type *base, const $acomp\_ladder\_config\_t *config)$ Set the voltage ladder configuration.$ 

# **Parameters**

- base ACOMP peripheral base address.
- config The structure for voltage ladder. If the config is NULL, voltage ladder would be diasbled, otherwise the voltage ladder would be configured and enabled.

FSL\_ACOMP\_DRIVER VERSION

ACOMP driver version 2.1.0.

enum \_acomp\_ladder\_reference\_voltage

The ACOMP ladder reference voltage.

Values:

```
enumerator kACOMP_LadderRefVoltagePinVDD
         Supply from pin VDD.
     enumerator kACOMP_LadderRefVoltagePinVDDCMP
         Supply from pin VDDCMP.
enum \_acomp\_interrupt\_enable
    The ACOMP interrupts enable.
     Values:
     enumerator kACOMP_InterruptsFallingEdgeEnable
         Enable the falling edge interrupts.
     enumerator~k ACOMP\_InterruptsRisingEdgeEnable
         Enable the rising edge interrupts.
     enumerator kACOMP InterruptsBothEdgesEnable
         Enable the both edges interrupts.
     enumerator kACOMP InterruptsDisable
         Disable the interrupts.
enum _acomp_hysteresis_selection
    The ACOMP hysteresis selection.
     Values:
     enumerator kACOMP_HysteresisNoneSelection
         None (the output will switch as the voltages cross).
    enumerator kACOMP_Hysteresis5MVSelection
         5mV.
     enumerator kACOMP Hysteresis10MVSelection
         10mV.
     enumerator kACOMP Hysteresis20MVSelection
         20mV.
typedef enum _acomp_ladder_reference_voltage acomp_ladder_reference_voltage_t
    The ACOMP ladder reference voltage.
typedef enum_acomp_interrupt_enable acomp_interrupt_enable_t
     The ACOMP interrupts enable.
typedef enum acomp hysteresis selection acomp hysteresis selection t
     The ACOMP hysteresis selection.
typedef struct acomp config acomp config t
    The structure for ACOMP basic configuration.
typedef struct _acomp_ladder_config acomp_ladder_config_t
    The structure for ACOMP voltage ladder.
struct _acomp_config
     #include <fsl_acomp.h> The structure for ACOMP basic configuration.
```

# **Public Members**

bool enableSyncToBusClk

If true, Comparator output is synchronized to the bus clock for output to other modules. If false, Comparator output is used directly.

acomp\_hysteresis\_selection\_t hysteresisSelection

Controls the hysteresis of the comparator.

```
struct \_acomp\_ladder\_config
```

#include <fsl\_acomp.h> The structure for ACOMP voltage ladder.

#### **Public Members**

```
uint8 t ladderValue
```

Voltage ladder value. 00000 = Vss, 00001 = 1\*Vref/31, ..., 11111 = Vref.

 $acomp\_ladder\_reference\_voltage\_t$  referenceVoltage

Selects the reference voltage(Vref) for the voltage ladder.

# 2.11 ADC: 12-bit SAR Analog-to-Digital Converter Driver

void ADC\_Init(ADC\_Type \*base, const adc\_config\_t \*config)

Initialize the ADC module.

#### **Parameters**

- base ADC peripheral base address.
- config Pointer to configuration structure, see to adc\_config\_t.

void ADC\_Deinit(ADC\_Type \*base)

Deinitialize the ADC module.

# **Parameters**

• base – ADC peripheral base address.

```
void ADC_GetDefaultConfig(adc_config_t *config)
```

Gets an available pre-defined settings for initial configuration.

This function initializes the initial configuration structure with an available settings. The default values are:

```
config->clockMode = kADC_ClockSynchronousMode;
config->clockDividerNumber = 0U;
config->resolution = kADC_Resolution12bit;
config->enableBypassCalibration = false;
config->sampleTimeNumber = 0U;
config->extendSampleTimeNumber = kADC_ExtendSampleTimeNotUsed;
```

#### **Parameters**

• config – Pointer to configuration structure.

static inline void ADC\_EnableConvSeqA(ADC\_Type \*base, bool enable)

Enable the conversion sequence A.

In order to avoid spuriously triggering the sequence, the trigger to conversion sequence should be ready before the sequence is ready. when the sequence is disabled, the trigger would be ignored. Also, it is suggested to disable the sequence during changing the sequence's setting.

#### **Parameters**

- base ADC peripheral base address.
- enable Switcher to enable the feature or not.

void  $ADC\_SetConvSeqAConfig(ADC\_Type *base, const $adc\_conv\_seq\_config\_t *config)$$  Configure the conversion sequence A.

#### **Parameters**

- base ADC peripheral base address.
- config Pointer to configuration structure, see to adc\_conv\_seq\_config\_t.

 $static\ in line\ void\ {\rm ADC\_DoSoftwareTriggerConvSeqA} (ADC\_Type\ *base)$ 

Do trigger the sequence's conversion by software.

#### **Parameters**

• base – ADC peripheral base address.

static inline void ADC\_EnableConvSeqABurstMode(ADC\_Type \*base, bool enable)

Enable the burst conversion of sequence A.

Enable the burst mode would cause the conversion sequence to be entinuously cycled through. Other triggers would be ignored while this mode is enabled. Repeated conversions could be halted by disabling this mode. And the sequence currently in process will be completed before enversions are terminated. Note that a new sequence could begin just before the burst mode is disabled.

#### **Parameters**

- base ADC peripheral base address.
- enable Switcher to enable this feature.

static inline void ADC\_SetConvSeqAHighPriority(ADC\_Type \*base)

Set the high priority for conversion sequence A.

# **Parameters**

• base – ADC peripheral bass address.

static inline void ADC\_EnableConvSeqB(ADC\_Type \*base, bool enable)

Enable the conversion sequence B.

In order to avoid spuriously triggering the sequence, the trigger to conversion sequence should be ready before the sequence is ready. when the sequence is disabled, the trigger would be ignored. Also, it is suggested to disable the sequence during changing the sequence's setting.

# **Parameters**

- base ADC peripheral base address.
- enable Switcher to enable the feature or not.

 $\label{local_conv} \begin{tabular}{ll} void ADC\_SetConvSeqBConfig(ADC\_Type *base, const $adc\_conv\_seq\_config\_t *config) \\ Configure the conversion sequence B. \end{tabular}$ 

# **Parameters**

- base ADC peripheral base address.
- config Pointer to configuration structure, see to add conv seg config t.

static inline void ADC DoSoftwareTriggerConvSeqB(ADC\_Type \*base)

Do trigger the sequence's conversion by software.

#### **Parameters**

• base – ADC peripheral base address.

static inline void ADC\_EnableConvSeqBBurstMode(ADC\_Type \*base, bool enable)

Enable the burst conversion of sequence B.

Enable the burst mode would cause the conversion sequence to be continuously cycled through. Other triggers would be ignored while this mode is enabled. Repeated conversions could be halted by disabling this mode. And the sequence currently in process will be completed before conversions are terminated. Note that a new sequence could begin just before the burst mode is disabled.

### **Parameters**

- base ADC peripheral base address.
- enable Switcher to enable this feature.

static inline void ADC\_SetConvSeqBHighPriority(ADC\_Type \*base)

Set the high priority for conversion sequence B.

#### **Parameters**

• base – ADC peripheral bass address.

bool ADC\_GetConvSeqAGlobalConversionResult(ADC\_Type \*base, adc\_result\_info\_t \*info) Get the global ADC conversion infomation of sequence A.

#### **Parameters**

- base ADC peripheral base address.
- info Pointer to information structure, see to adc\_result\_info\_t;

### **Return values**

- true The conversion result is ready.
- false The conversion result is not ready yet.

 $bool\ ADC\_GetConvSeqBGlobalConversionResult(ADC\_Type\ *base,\ adc\_result\_info\_t\ *info)$  Get the global ADC conversion infomation of sequence B.

# **Parameters**

- base ADC peripheral base address.
- info Pointer to information structure, see to adc\_result\_info\_t;

# **Return values**

- true The conversion result is ready.
- false The conversion result is not ready yet.

bool ADC\_GetChannelConversionResult(ADC\_Type \*base, uint32\_t channel, adc\_result\_info\_t \*info)

Get the channel's ADC conversion completed under each conversion sequence.

### **Parameters**

- base ADC peripheral base address.
- channel The indicated channel number.
- info Pointer to information structure, see to adc\_result\_info\_t;

## **Return values**

- true The conversion result is ready.
- false The conversion result is not ready yet.

static inline void ADC\_SetThresholdPair0(ADC\_Type \*base, uint32\_t lowValue, uint32\_t highValue)

Set the threshhold pair 0 with low and high value.

#### **Parameters**

- base ADC peripheral base address.
- lowValue LOW threshold value.
- highValue HIGH threshold value.

static inline void ADC\_SetThresholdPair1(ADC\_Type \*base, uint32\_t lowValue, uint32\_t highValue)

Set the threshhold pair 1 with low and high value.

#### **Parameters**

- base ADC peripheral base address.
- lowValue LOW threshold value. The available value is with 12-bit.
- highValue HIGH threshold value. The available value is with 12-bit.

static inline void ADC\_SetChannelWithThresholdPair0(ADC\_Type \*base, uint32\_t channelMask) Set given channels to apply the threshold pare 0.

#### **Parameters**

- base ADC peripheral base address.
- channelMask Indicated channels' mask.

 $static\ in line\ void\ {\rm ADC\_SetChannelWithThresholdPair1} (ADC\_Type\ *base,\ uint 32\_t\ channelMask)\\ Set\ given\ channels\ to\ apply\ the\ threshold\ pare\ 1.$ 

## **Parameters**

- base ADC peripheral base address.
- channelMask Indicated channels' mask.

static inline void ADC EnableInterrupts(ADC\_Type \*base, uint32\_t mask)

Enable interrupts for conversion sequences.

# **Parameters**

- base ADC peripheral base address.
- mask Mask of interrupt mask value for global block except each channal, see to \_adc\_interrupt\_enable.

static inline void ADC DisableInterrupts(ADC\_Type \*base, uint32\_t mask)

Disable interrupts for conversion sequence.

# **Parameters**

- base ADC peripheral base address.
- mask Mask of interrupt mask value for global block except each channel, see to \_adc\_interrupt\_enable.

 $static\ in line\ void\ ADC\_Enable Threshold Compare Interrupt (ADC\_Type\ *base,\ uint 32\_t\ channel,\\ adc\_threshold\_interrupt\_mode\_t\ mode)$ 

Enable the interrupt of threshold compare event for each channel.

## **Parameters**

- base ADC peripheral base address.
- channel Channel number.
- mode Interrupt mode for threshold compare event, see to adc\_threshold\_interrupt\_mode\_t.

static inline uint32\_t ADC\_GetStatusFlags(ADC\_Type \*base) Get status flags of ADC module.

#### **Parameters**

• base – ADC peripheral base address.

# **Returns**

Mask of status flags of module, see to \_adc\_status\_flags.

 $static\ in line\ void\ {\rm ADC\_ClearStatusFlags}(ADC\_Type\ *base,\ uint 32\_t\ mask)\\ Clear\ status\ flags\ of\ ADC\ module.$ 

#### **Parameters**

- base ADC peripheral base address.
- mask Mask of status flags of module, see to \_adc\_status\_flags.

FSL\_ADC\_DRIVER\_VERSION ADC driver version 2.6.0.

 $enum \_adc\_status\_flags$ 

Flags.

Values:

enumerator kADC\_ThresholdCompareFlagOnChn0

Threshold comparison event on Channel 0.

 ${\bf enumerator}~{\rm kADC\_ThresholdCompareFlagOnChn1}$ 

Threshold comparison event on Channel 1.

 ${\bf enumerator~kADC\_ThresholdCompareFlagOnChn2}$ 

Threshold comparison event on Channel 2.

enumerator kADC\_ThresholdCompareFlagOnChn3 Threshold comparison event on Channel 3.

enumerator kADC ThresholdCompareFlagOnChn4

Threshold comparison event on Channel 4.

 ${\bf enumerator}~{\rm kADC\_ThresholdCompareFlagOnChn5}$ 

Threshold comparison event on Channel 5.

 $enumerator~\mathrm{kADC\_ThresholdCompareFlagOnChn6}$ 

Threshold comparison event on Channel 6.

 $enumerator~k ADC\_Threshold Compare Flag On Chn7$ 

Threshold comparison event on Channel 7.

 ${\bf enumerator}~{\rm kADC\_ThresholdCompareFlagOnChn8}$ 

Threshold comparison event on Channel 8.

 ${\bf enumerator} \ {\rm kADC\_ThresholdCompareFlagOnChn9}$ 

Threshold comparison event on Channel 9.

 ${\bf enumerator}~{\rm kADC\_ThresholdCompareFlagOnChn10}$ 

Threshold comparison event on Channel 10.

enumerator kADC\_ThresholdCompareFlagOnChn11

```
Threshold comparison event on Channel 11.
     enumerator kADC_OverrunFlagForChn0
         Mirror the OVERRUN status flag from the result register for ADC channel 0.
     enumerator kADC OverrunFlagForChn1
         Mirror the OVERRUN status flag from the result register for ADC channel 1.
     enumerator kADC_OverrunFlagForChn2
         Mirror the OVERRUN status flag from the result register for ADC channel 2.
     enumerator kADC_OverrunFlagForChn3
         Mirror the OVERRUN status flag from the result register for ADC channel 3.
     enumerator kADC OverrunFlagForChn4
         Mirror the OVERRUN status flag from the result register for ADC channel 4.
     enumerator kADC OverrunFlagForChn5
         Mirror the OVERRUN status flag from the result register for ADC channel 5.
     enumerator kADC OverrunFlagForChn6
         Mirror the OVERRUN status flag from the result register for ADC channel 6.
     enumerator kADC OverrunFlagForChn7
         Mirror the OVERRUN status flag from the result register for ADC channel 7.
     enumerator kADC OverrunFlagForChn8
         Mirror the OVERRUN status flag from the result register for ADC channel 8.
     enumerator kADC_OverrunFlagForChn9
         Mirror the OVERRUN status flag from the result register for ADC channel 9.
     enumerator kADC_OverrunFlagForChn10
         Mirror the OVERRUN status flag from the result register for ADC channel 10.
     enumerator kADC OverrunFlagForChn11
         Mirror the OVERRUN status flag from the result register for ADC channel 11.
     enumerator kADC_GlobalOverrunFlagForSeqA
         Mirror the glabal OVERRUN status flag for conversion sequence A.
     enumerator kADC_GlobalOverrunFlagForSeqB
         Mirror the global OVERRUN status flag for conversion sequence B.
     enumerator kADC ConvSeqAInterruptFlag
         Sequence A interrupt/DMA trigger.
     enumerator kADC ConvSeqBInterruptFlag
         Sequence B interrupt/DMA trigger.
     enumerator kADC_ThresholdCompareInterruptFlag
         Threshold comparision interrupt flag.
     enumerator kADC_OverrunInterruptFlag
         Overrun interrupt flag.
enum adc interrupt enable
    Interrupts.
    Note: Not all the interrupt options are listed here
     Values:
```

```
enumerator kADC ConvSeqAInterruptEnable
```

Enable interrupt upon completion of each individual conversion in sequence A, or entire sequence.

enumerator kADC\_ConvSeqBInterruptEnable

Enable interrupt upon completion of each individual conversion in sequence B, or entire sequence.

enumerator kADC\_OverrunInterruptEnable

Enable the detection of an overrun condition on any of the channel data registers will cause an overrun interrupt/DMA trigger.

 $enum \_ adc\_ clock\_ mode$ 

Define selection of clock mode.

Values:

enumerator kADC ClockSynchronousMode

The ADC clock would be derived from the system clock based on "clockDividerNumber".

enumerator kADC\_ClockAsynchronousMode

The ADC clock would be based on the SYSCON block's divider.

 $enum \_adc\_resolution$ 

Define selection of resolution.

Values:

enumerator kADC Resolution6bit

6-bit resolution.

 $enumerator~\mathrm{kADC\_Resolution8bit}$ 

8-bit resolution.

enumerator kADC Resolution10bit

10-bit resolution.

enumerator kADC Resolution12bit

12-bit resolution.

enum adc voltage range

Definfe range of the analog supply voltage VDDA.

Values.

 $enumerator~kADC\_HighVoltageRange$ 

enumerator kADC\_LowVoltageRange

enum \_adc\_trigger\_polarity

Define selection of polarity of selected input trigger for conversion sequence.

Values:

enumerator kADC TriggerPolarityNegativeEdge

A negative edge launches the conversion sequence on the trigger(s).

enumerator kADC TriggerPolarityPositiveEdge

A positive edge launches the conversion sequence on the trigger(s).

enum adc priority

Define selection of conversion sequence's priority.

Values:

enumerator kADC PriorityLow

```
This sequence would be preempted when another sequence is started.
     enumerator kADC PriorityHigh
         This sequence would preempt other sequence even when it is started.
enum _adc_seq_interrupt_mode
     Define selection of conversion sequence's interrupt.
     Values:
     enumerator kADC InterruptForEachConversion
         The sequence interrupt/DMA trigger will be set at the end of each individual ADC con-
         version inside this conversion sequence.
     enumerator kADC InterruptForEachSequence
         The sequence interrupt/DMA trigger will be set when the entire set of this sequence
         conversions completes.
enum adc threshold compare status
     Define status of threshold compare result.
     Values:
     enumerator kADC ThresholdCompareInRange
         LOW threshold <= conversion value <= HIGH threshold.
     enumerator \ \mathrm{kADC\_ThresholdCompareBelowRange}
         conversion value < LOW threshold.
     enumerator \ kADC\_ThresholdCompareAboveRange
         conversion value > HIGH threshold.
enum _adc_threshold_crossing_status
     Define status of threshold crossing detection result.
     Values:
     enumerator kADC ThresholdCrossingNoDetected
         No threshold Crossing detected.
     enumerator kADC_ThresholdCrossingDownward
         Downward Threshold Crossing detected.
     enumerator kADC ThresholdCrossingUpward
         Upward Threshold Crossing Detected.
enum adc threshold interrupt mode
     Define interrupt mode for threshold compare event.
     Values:
     enumerator kADC ThresholdInterruptDisabled
         Threshold comparison interrupt is disabled.
     enumerator kADC ThresholdInterruptOnOutside
         Threshold comparison interrupt is enabled on outside threshold.
     enumerator kADC ThresholdInterruptOnCrossing
         Threshold comparison interrupt is enabled on crossing threshold.
enum adc inforesultshift
     Define the info result mode of different resolution.
     Values:
```

```
enumerator kADC Resolution12bitInfoResultShift
         Info result shift of Resolution12bit.
     enumerator kADC Resolution10bitInfoResultShift
         Info result shift of Resolution10bit.
     enumerator kADC Resolution8bitInfoResultShift
         Info result shift of Resolution8bit.
     enumerator kADC Resolution6bitInfoResultShift
         Info result shift of Resolution6bit.
enum adc tempsensor common mode
    Define common modes for Temerature sensor.
     Values:
     enumerator kADC HighNegativeOffsetAdded
         Temperature sensor common mode: high negative offset added.
     enumerator kADC IntermediateNegativeOffsetAdded
         Temperature sensor common mode: intermediate negative offset added.
     enumerator kADC NoOffsetAdded
         Temperature sensor common mode: no offset added.
     enumerator kADC LowPositiveOffsetAdded
         Temperature sensor common mode: low positive offset added.
enum adc second control
    Define source impedance modes for GPADC control.
     Values:
     enumerator kADC Impedance621Ohm
         Extand ADC sampling time according to source impedance 1: 0.621 kOhm.
     enumerator kADC Impedance55kOhm
         Extand ADC sampling time according to source impedance 20 (default): 55 kOhm.
     enumerator kADC Impedance87kOhm
         Extand ADC sampling time according to source impedance 31: 87 kOhm.
     enumerator kADC NormalFunctionalMode
         TEST mode: Normal functional mode.
     enumerator kADC MultiplexeTestMode
         TEST mode: Multiplexer test mode.
     enumerator kADC ADCInUnityGainMode
         TEST mode: ADC in unity gain mode.
typedef enum adc clock mode adc clock mode t
     Define selection of clock mode.
typedef enum _adc_resolution adc resolution t
    Define selection of resolution.
typedef enum_adc_voltage_range adc_vdda_range_t
     Definfe range of the analog supply voltage VDDA.
typedef enum _adc_trigger_polarity adc trigger polarity t
    Define selection of polarity of selected input trigger for conversion sequence.
```

```
typedef enum _adc_priority adc_priority_t
     Define selection of conversion sequence's priority.
typedef enum _adc_seq_interrupt_mode adc_seq_interrupt_mode_t
     Define selection of conversion sequence's interrupt.
typedef enum _adc_threshold_compare_status adc_threshold_compare_status_t
     Define status of threshold compare result.
typedef enum adc threshold crossing status adc threshold crossing status t
     Define status of threshold crossing detection result.
typedef enum _adc_threshold_interrupt_mode adc threshold interrupt mode t
     Define interrupt mode for threshold compare event.
typedef enum _adc_inforesultshift adc inforesult t
     Define the info result mode of different resolution.
typedef enum _adc_tempsensor_common_mode adc_tempsensor_common_mode_t
     Define common modes for Temerature sensor.
typedef enum _adc_second_control adc second control t
     Define source impedance modes for GPADC control.
typedef struct _adc_config adc_config_t
     Define structure for configuring the block.
typedef struct_adc_conv_seq_config adc_conv_seq_config_t
     Define structure for configuring conversion sequence.
typedef struct _adc_result_info adc_result_info_t
     Define structure of keeping conversion result information.
struct adc config
```

# **Public Members**

adc clock mode t clockMode

Select the clock mode for ADC converter.

#include <fsl adc.h> Define structure for configuring the block.

uint32 t clockDividerNumber

This field is only available when using kADC\_ClockSynchronousMode for "clockMode" field. The divider would be plused by 1 based on the value in this field. The available range is in 8 bits.

 $adc\_resolution\_t$  resolution

Select the conversion bits.

 ${\color{blue}bool\ enable Bypass Calibration}$ 

By default, a calibration cycle must be performed each time the chip is powered-up. Re-calibration may be warranted periodically - especially if operating conditions have changed. To enable this option would avoid the need to calibrate if offset error is not a concern in the application.

 $uint32\_t$  sampleTimeNumber

By default, with value as "0U", the sample period would be 2.5 ADC clocks. Then, to plus the "sampleTimeNumber" value here. The available value range is in 3 bits.

# bool enableLowPowerMode

If disable low-power mode, ADC remains activated even when no conversions are requested. If enable low-power mode, The ADC is automatically powered-down when no conversions are taking place.

# adc\_vdda\_range\_t voltageRange

Configure the ADC for the appropriate operating range of the analog supply voltage VDDA. Failure to set the area correctly causes the ADC to return incorrect conversion results.

```
struct \_adc\_conv\_seq\_config
```

#include <fsl\_adc.h> Define structure for configuring conversion sequence.

#### **Public Members**

# $uint32\_t$ channelMask

Selects which one or more of the ADC channels will be sampled and converted when this sequence is launched. The masked channels would be involved in current conversion sequence, beginning with the lowest-order. The available range is in 12-bit.

## uint32\_t triggerMask

Selects which one or more of the available hardware trigger sources will cause this conversion sequence to be initiated. The available range is 6-bit.

# adc\_trigger\_polarity\_t triggerPolarity

Select the trigger to launch conversion sequence.

# bool enableSyncBypass

To enable this feature allows the hardware trigger input to bypass synchronization flip-flop stages and therefore shorten the time between the trigger input signal and the start of a conversion.

# bool enableSingleStep

When enabling this feature, a trigger will launch a single conversion on the next channel in the sequence instead of the default response of launching an entire sequence of conversions.

### adc seg interrupt mode t interruptMode

Select the interrpt/DMA trigger mode.

```
struct adc result info
```

#include <fsl\_adc.h> Define structure of keeping conversion result information.

#### **Public Members**

uint32 t result

Keep the conversion data value.

 $adc\_threshold\_compare\_status\_t \ {\it thresholdCompareStatus}$ 

Keep the threshold compare status.

 $adc\_threshold\_crossing\_status\_t \ thresholdCorssingStatus$ 

Keep the threshold crossing status.

# $uint32\_t$ channelNumber

Keep the channel number for this conversion.

# bool overrunFlag

Keep the status whether the conversion is overrun or not.

# 2.12 GPIO: General Purpose I/O

void GPIO\_PortInit(GPIO\_Type \*base, uint32\_t port)

Initializes the GPIO peripheral.

This function ungates the GPIO clock.

### **Parameters**

- base GPIO peripheral base pointer.
- port GPIO port number.

void GPIO\_PinInit(GPIO\_Type \*base, uint32\_t port, uint32\_t pin, const *gpio\_pin\_config\_t* \*config)

Initializes a GPIO pin used by the board.

To initialize the GPIO, define a pin configuration, either input or output, in the user file. Then, call the GPIO PinInit() function.

This is an example to define an input pin or output pin configuration:

```
Define a digital input pin configuration,
gpio_pin_config_t config =

{
    kGPIO_DigitalInput,
    0,
}
Define a digital output pin configuration,
gpio_pin_config_t config =

{
    kGPIO_DigitalOutput,
    0,
}
```

# **Parameters**

- base GPIO peripheral base pointer(Typically GPIO)
- port GPIO port number
- pin GPIO pin number
- config GPIO pin configuration pointer

 $static\ in line\ void\ {\rm GPIO\_PinWrite}(GPIO\_Type\ *base,\ uint 32\_t\ port,\ uint 32\_t\ pin,\ uint 8\_t\ output)$  Sets the output level of the one GPIO pin to the logic 1 or 0.

#### **Parameters**

- base GPIO peripheral base pointer(Typically GPIO)
- port GPIO port number
- pin GPIO pin number
- output GPIO pin output logic level.
  - 0: corresponding pin output low-logic level.
  - 1: corresponding pin output high-logic level.

static inline uint32\_t  $\mathrm{GPIO}_{\mathrm{PinRead}}(\mathrm{GPIO}_{\mathrm{Type}}$  \*base, uint32\_t port, uint32\_t pin) Reads the current input value of the GPIO PIN.

#### **Parameters**

• base – GPIO peripheral base pointer(Typically GPIO)

- port GPIO port number
- pin GPIO pin number

# **Return values**

GPIO – port input value

- 0: corresponding pin input low-logic level.
- 1: corresponding pin input high-logic level.

FSL\_GPIO\_DRIVER\_VERSION

LPC GPIO driver version.

enum gpio pin direction

LPC GPIO direction definition.

Values:

enumerator kGPIO DigitalInput

Set current pin as digital input

enumerator kGPIO DigitalOutput

Set current pin as digital output

typedef enum \_gpio\_pin\_direction gpio\_pin\_direction\_t

LPC GPIO direction definition.

typedef struct \_gpio\_pin\_config gpio\_pin\_config\_t

The GPIO pin configuration structure.

Every pin can only be configured as either output pin or input pin at a time. If configured as a input pin, then leave the outputConfig unused.

static inline void GPIO\_PortSet(GPIO\_Type \*base, uint32\_t port, uint32\_t mask)

Sets the output level of the multiple GPIO pins to the logic 1.

### **Parameters**

- base GPIO peripheral base pointer(Typically GPIO)
- port GPIO port number
- mask GPIO pin number macro

static inline void GPIO\_PortClear(GPIO\_Type \*base, uint32\_t port, uint32\_t mask)

Sets the output level of the multiple GPIO pins to the logic 0.

# **Parameters**

- base GPIO peripheral base pointer(Typically GPIO)
- port GPIO port number
- mask GPIO pin number macro

static inline void GPIO\_PortToggle(GPIO\_Type \*base, uint32\_t port, uint32\_t mask)

Reverses current output logic of the multiple GPIO pins.

# **Parameters**

- base GPIO peripheral base pointer(Typically GPIO)
- port GPIO port number
- mask GPIO pin number macro

```
struct _gpio_pin_config
```

#include <fsl\_gpio.h> The GPIO pin configuration structure.

Every pin can only be configured as either output pin or input pin at a time. If configured as a input pin, then leave the outputConfig unused.

## **Public Members**

```
gpio_pin_direction_t pinDirection
GPIO direction, input or output
uint8_t outputLogic
Set default output logic, no use in input
```

# 2.13 IOCON: I/O pin configuration

```
LPC_IOCON_DRIVER_VERSION
```

IOCON driver version 2.0.2.

typedef struct \_iocon\_group iocon\_group\_t

Array of IOCON pin definitions passed to IOCON\_SetPinMuxing() must be in this format.

```
___STATIC_INLINE void IOCON_PinMuxSet (IOCON_Type *base, uint8_t ionumber, uint32_t modefunc)
```

IOCON function and mode selection definitions.

Sets I/O Control pin mux

Note: See the User Manual for specific modes and functions supported by the various pins.

#### **Parameters**

- base : The base of IOCON peripheral on the chip
- ionumber -: GPIO number to mux
- modefunc -: OR'ed values of type IOCON\_\*

# **Returns**

Nothing

```
__STATIC_INLINE void IOCON_SetPinMuxing (IOCON_Type *base, const iocon_group_t *pinArray, uint32_t arrayLength)
```

Set all I/O Control pin muxing.

#### **Parameters**

- base : The base of IOCON peripheral on the chip
- pinArray -: Pointer to array of pin mux selections
- arrayLength –: Number of entries in pinArray

### **Returns**

Nothing

FSL COMPONENT ID

 $struct \_iocon\_group$ 

#include <fsl\_iocon.h> Array of IOCON pin definitions passed to IOCON\_SetPinMuxing() must be in this format.

# 2.14 MRT: Multi-Rate Timer

void MRT Init(MRT\_Type \*base, const mrt\_config\_t \*config)

Ungates the MRT clock and configures the peripheral for basic operation.

**Note:** This API should be called at the beginning of the application using the MRT driver.

### **Parameters**

- base Multi-Rate timer peripheral base address
- config Pointer to user's MRT config structure. If MRT has MULTITASK bit field in MODCFG reigster, param config is useless.

 $void \ \mathrm{MRT\_Deinit}(MRT\_Type \ *base)$ 

Gate the MRT clock.

#### **Parameters**

• base – Multi-Rate timer peripheral base address

static inline void MRT GetDefaultConfig(mrt\_config\_t \*config)

Fill in the MRT config struct with the default settings.

The default values are:

config->enableMultiTask = false;

# **Parameters**

• config – Pointer to user's MRT config structure.

static inline void MRT\_SetupChannelMode(MRT\_Type \*base,  $mrt\_chnl\_t$  channel, const  $mrt\_timer\_mode\_t$  mode)

Sets up an MRT channel mode.

# **Parameters**

- base Multi-Rate timer peripheral base address
- channel Channel that is being configured.
- mode Timer mode to use for the channel.

 $static\ in line\ void\ \mathrm{MRT\_EnableInterrupts}(\mathbf{MRT\_Type}\ *base,\ \mathit{mrt\_chnl\_t}\ channel,\ uint 32\_t\ mask)\\ Enables\ the\ \mathsf{MRT}\ interrupt.$ 

# **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number
- $\bullet \; {\rm mask}$  The interrupts to enable. This is a logical OR of members of the enumeration mrt\_interrupt\_enable\_t

static inline void  $MRT\_DisableInterrupts(MRT\_Type *base, mrt\_chnl\_t channel, uint32\_t mask)$  Disables the selected MRT interrupt.

#### **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number
- mask The interrupts to disable. This is a logical OR of members of the enumeration mrt\_interrupt\_enable\_t

static inline uint32\_t  $MRT\_GetEnabledInterrupts(MRT\_Type *base, mrt\_chnl\_t channel)$  Gets the enabled MRT interrupts.

#### **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number

#### **Returns**

The enabled interrupts. This is the logical OR of members of the enumeration mrt\_interrupt\_enable\_t

static inline uint32\_t  $MRT\_GetStatusFlags(MRT\_Type *base, mrt\_chnl\_t channel)$  Gets the MRT status flags.

#### **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number

### **Returns**

The status flags. This is the logical OR of members of the enumeration mrt status flags t

 $static\ in line\ void\ \mathrm{MRT\_ClearStatusFlags}(\mathbf{MRT\_Type}\ *base,\ \mathit{mrt\_chnl\_t}\ channel,\ uint 32\_t\ mask)$  Clears the MRT status\ flags.

# **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number
- $\bullet$   ${\rm mask}$  The status flags to clear. This is a logical OR of members of the enumeration mrt\_status\_flags\_t

 $\begin{tabular}{ll} {\bf Void\ MRT\_UpdateTimerPeriod}({\bf MRT\_Type\ *base}, {\it mrt\_chnl\_t\ channel,\ uint32\_t\ count,\ bool\ immediateLoad}) \end{tabular}$ 

Used to update the timer period in units of count.

The new value will be immediately loaded or will be loaded at the end of the current time interval. For one-shot interrupt mode the new value will be immediately loaded.

Note: User can call the utility macros provided in fsl\_common.h to convert to ticks

### **Parameters**

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- base Multi-Rate timer peripheral base address
- channel Timer channel number
- count Timer period in units of ticks

• immediateLoad – true: Load the new value immediately into the TIMER register; false: Load the new value at the end of current timer interval

 $static\ in line\ uint 32\_t\ \mathrm{MRT\_GetCurrentTimerCount}(MRT\_Type\ *base, \textit{mrt\_chnl\_t}\ channel)$ 

Reads the current timer counting value.

This function returns the real-time timer counting value, in a range from 0 to a timer period.

**Note:** User can call the utility macros provided in fsl\_common.h to convert ticks to usec or msec

### **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number

#### **Returns**

Current timer counting value in ticks

static inline void  $MRT\_StartTimer(MRT\_Type *base, mrt\_chnl\_t channel, uint32\_t count)$  Starts the timer counting.

After calling this function, timers load period value, counts down to 0 and depending on the timer mode it will either load the respective start value again or stop.

**Note:** User can call the utility macros provided in fsl\_common.h to convert to ticks

### **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number.
- count Timer period in units of ticks. Count can contain the LOAD bit, which control the force load feature.

static inline void MRT\_StopTimer(MRT\_Type \*base, *mrt\_chnl\_t* channel)

Stops the timer counting.

This function stops the timer from counting.

# **Parameters**

- base Multi-Rate timer peripheral base address
- channel Timer channel number.

static inline uint32\_t MRT\_GetIdleChannel(MRT\_Type \*base)

Find the available channel.

This function returns the lowest available channel number.

#### **Parameters**

• base – Multi-Rate timer peripheral base address

FSL MRT DRIVER VERSION

 $enum \_ \mathrm{mrt} \_ \mathrm{chnl}$ 

List of MRT channels.

Values:

```
enumerator kMRT\_Channel\_0
         MRT channel number 0
     enumerator kMRT Channel 1
         MRT channel number 1
     enumerator kMRT Channel 2
         MRT channel number 2
     enumerator kMRT Channel 3
         MRT channel number 3
enum \_ mrt\_ timer\_ mode
    List of MRT timer modes.
     Values:
     enumerator kMRT RepeatMode
         Repeat Interrupt mode
     enumerator kMRT OneShotMode
         One-shot Interrupt mode
     enumerator kMRT OneShotStallMode
         One-shot stall mode
enum mrt interrupt enable
    List of MRT interrupts.
     Values:
     enumerator kMRT TimerInterruptEnable
         Timer interrupt enable
enum _mrt_status_flags
    List of MRT status flags.
     Values:
     enumerator kMRT_TimerInterruptFlag
         Timer interrupt flag
     enumerator kMRT TimerRunFlag
         Indicates state of the timer
typedef enum _mrt_chnl mrt chnl t
    List of MRT channels.
typedef enum mrt timer mode mrt timer mode t
     List of MRT timer modes.
typedef enum mrt interrupt enable mrt interrupt enable t
    List of MRT interrupts.
typedef enum _mrt_status_flags mrt_status_flags_t
    List of MRT status flags.
typedef struct _mrt_config mrt config t
    MRT configuration structure.
    This structure holds the configuration settings for the MRT peripheral. To initialize this
    structure to reasonable defaults, call the MRT_GetDefaultConfig() function and pass a
    pointer to your config structure instance.
```

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The config struct can be made const so it resides in flash

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```
struct _mrt_config
```

#include <fsl\_mrt.h> MRT configuration structure.

This structure holds the configuration settings for the MRT peripheral. To initialize this structure to reasonable defaults, call the MRT\_GetDefaultConfig() function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

#### **Public Members**

bool enableMultiTask

true: Timers run in multi-task mode; false: Timers run in hardware status mode

# 2.15 PINT: Pin Interrupt and Pattern Match Driver

```
FSL_PINT_DRIVER_VERSION
enum \_ pint\_ pin\_ enable
    PINT Pin Interrupt enable type.
     Values:
     enumerator kPINT PinIntEnableNone
         Do not generate Pin Interrupt
     enumerator kPINT PinIntEnableRiseEdge
         Generate Pin Interrupt on rising edge
    enumerator kPINT PinIntEnableFallEdge
         Generate Pin Interrupt on falling edge
     enumerator kPINT PinIntEnableBothEdges
         Generate Pin Interrupt on both edges
     enumerator kPINT PinIntEnableLowLevel
         Generate Pin Interrupt on low level
     enumerator kPINT PinIntEnableHighLevel
         Generate Pin Interrupt on high level
enum pint int
    PINT Pin Interrupt type.
     Values:
     enumerator kPINT PinInt0
         Pin Interrupt 0
enum _pint_pmatch_input_src
    PINT Pattern Match bit slice input source type.
     Values:
     enumerator kPINT_PatternMatchInp0Src
         Input source 0
     enumerator kPINT_PatternMatchInp1Src
         Input source 1
```

```
{\bf enumerator} \; {\rm kPINT\_PatternMatchInp2Src}
         Input source 2
     enumerator kPINT_PatternMatchInp3Src
         Input source 3
     enumerator kPINT_PatternMatchInp4Src
         Input source 4
     enumerator kPINT_PatternMatchInp5Src
         Input source 5
     enumerator kPINT PatternMatchInp6Src
         Input source 6
     enumerator kPINT_PatternMatchInp7Src
         Input source 7
     {\bf enumerator} \ kPINT\_SecPatternMatchInp0Src
         Input source 0
     enumerator kPINT_SecPatternMatchInp1Src
         Input source 1
enum _pint_pmatch_bslice
     PINT Pattern Match bit slice type.
     Values:
     enumerator kPINT PatternMatchBSlice0
         Bit slice 0
enum _pint_pmatch_bslice_cfg
     PINT Pattern Match configuration type.
     Values:
     enumerator kPINT PatternMatchAlways
         Always Contributes to product term match
     enumerator kPINT PatternMatchStickyRise
         Sticky Rising edge
     enumerator kPINT PatternMatchStickyFall
         Sticky Falling edge
     enumerator kPINT PatternMatchStickyBothEdges
         Sticky Rising or Falling edge
     enumerator kPINT_PatternMatchHigh
         High level
     enumerator kPINT_PatternMatchLow
         Low level
     enumerator kPINT PatternMatchNever
         Never contributes to product term match
     enumerator kPINT PatternMatchBothEdges
         Either rising or falling edge
typedef enum _pint_pin_enable pint pin enable t
     PINT Pin Interrupt enable type.
```

```
typedef enum _pint_int pint_pin_int_t
```

PINT Pin Interrupt type.

typedef enum \_pint\_pmatch\_input\_src pint\_pmatch\_input\_src\_t

PINT Pattern Match bit slice input source type.

typedef enum \_pint\_pmatch\_bslice pint\_pmatch\_bslice\_t

PINT Pattern Match bit slice type.

typedef enum \_pint\_pmatch\_bslice\_cfg pint\_pmatch\_bslice\_cfg\_t

PINT Pattern Match configuration type.

typedef struct \_pint\_status pint\_status\_t

PINT event status.

typedef void (\*pint\_cb\_t)(pint\_pin\_int\_t pintr, pint\_status\_t \*status)

PINT Callback function.

 $typedef\ struct\_pint\_pmatch\_cfg\ \operatorname{pint\_pmatch\_cfg\_t}$ 

void PINT Init(PINT\_Type \*base)

Initialize PINT peripheral.

This function initializes the PINT peripheral and enables the clock.

#### **Parameters**

• base – Base address of the PINT peripheral.

## **Return values**

None. -

void PINT\_SetCallback(PINT\_Type \*base, pint\_cb\_t callback)

Set PINT callback.

This function set the callback for PINT interupt handler.

# **Parameters**

- base Base address of the PINT peripheral.
- callback Callback.

# **Return values**

None. -

void PINT\_PinInterruptConfig(PINT\_Type \*base, pint\_pin\_int\_t intr, pint\_pin\_enable\_t enable) Configure PINT peripheral pin interrupt.

This function configures a given pin interrupt.

# **Parameters**

- base Base address of the PINT peripheral.
- intr Pin interrupt.
- enable Selects detection logic.

# **Return values**

None. -

Get PINT peripheral pin interrupt configuration.

This function returns the configuration of a given pin interrupt.

#### **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.
- enable Pointer to store the detection logic.

#### **Return values**

None. -

void PINT\_PinInterruptClrStatus(PINT\_Type \*base, pint\_pin\_int\_t pintr)

Clear Selected pin interrupt status only when the pin was triggered by edge-sensitive.

This function clears the selected pin interrupt status.

# **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.

# **Return values**

None. -

static inline uint32\_t PINT\_PinInterruptGetStatus(PINT\_Type \*base, pint\_pin\_int\_t pintr) Get Selected pin interrupt status.

This function returns the selected pin interrupt status.

#### **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.

#### **Return values**

status – = 0 No pin interrupt request. = 1 Selected Pin interrupt request active.

void PINT\_PinInterruptClrStatusAll(PINT\_Type \*base)

Clear all pin interrupts status only when pins were triggered by edge-sensitive.

This function clears the status of all pin interrupts.

# **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

None. -

static inline uint32\_t PINT\_PinInterruptGetStatusAll(PINT\_Type \*base)

Get all pin interrupts status.

This function returns the status of all pin interrupts.

# **Parameters**

• base – Base address of the PINT peripheral.

# Return values

status – Each bit position indicates the status of corresponding pin interrupt.

= 0 No pin interrupt request. = 1 Pin interrupt request active.

static inline void PINT\_PinInterruptClrFallFlag(PINT\_Type \*base, pint\_pin\_int\_t pintr)

Clear Selected pin interrupt fall flag.

This function clears the selected pin interrupt fall flag.

# **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.

# **Return values**

None. -

static inline uint32\_t PINT\_PinInterruptGetFallFlag(PINT\_Type \*base, pint\_pin\_int\_t pintr) Get selected pin interrupt fall flag.

This function returns the selected pin interrupt fall flag.

#### **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.

# **Return values**

flag - = 0 Falling edge has not been detected. = 1 Falling edge has been detected.

static inline void PINT\_PinInterruptClrFallFlagAll(PINT\_Type \*base)

Clear all pin interrupt fall flags.

This function clears the fall flag for all pin interrupts.

#### **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

None. -

static inline uint32\_t PINT\_PinInterruptGetFallFlagAll(PINT\_Type \*base)

Get all pin interrupt fall flags.

This function returns the fall flag of all pin interrupts.

## **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

 ${
m flags}$  – Each bit position indicates the falling edge detection of the corresponding pin interrupt. 0 Falling edge has not been detected. = 1 Falling edge has been detected.

static inline void PINT\_PinInterruptClrRiseFlag(PINT\_Type \*base, pint\_pin\_int\_t pintr) Clear Selected pin interrupt rise flag.

This function clears the selected pin interrupt rise flag.

#### **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.

# Return values

None. -

static inline uint $32_t$  PINT\_PinInterruptGetRiseFlag(PINT\_Type \*base,  $pint_pin_int_t$  pintr) Get selected pin interrupt rise flag.

This function returns the selected pin interrupt rise flag.

#### **Parameters**

- base Base address of the PINT peripheral.
- pintr Pin interrupt.

# **Return values**

 ${
m flag}$  – = 0 Rising edge has not been detected. = 1 Rising edge has been detected.

static inline void PINT PinInterruptClrRiseFlagAll(PINT\_Type \*base)

Clear all pin interrupt rise flags.

This function clears the rise flag for all pin interrupts.

#### **Parameters**

• base – Base address of the PINT peripheral.

#### **Return values**

None. -

static inline uint32\_t PINT\_PinInterruptGetRiseFlagAll(PINT\_Type \*base)

Get all pin interrupt rise flags.

This function returns the rise flag of all pin interrupts.

#### **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

flags – Each bit position indicates the rising edge detection of the corresponding pin interrupt. 0 Rising edge has not been detected. = 1 Rising edge has been detected.

void PINT\_PatternMatchConfig(PINT\_Type \*base, pint\_pmatch\_bslice\_t bslice, pint\_pmatch\_cfg\_t \*cfg)

Configure PINT pattern match.

This function configures a given pattern match bit slice.

#### **Parameters**

- base Base address of the PINT peripheral.
- bslice Pattern match bit slice number.
- cfg Pointer to bit slice configuration.

#### **Return values**

None. -

Get PINT pattern match configuration.

This function returns the configuration of a given pattern match bit slice.

# **Parameters**

- base Base address of the PINT peripheral.
- bslice Pattern match bit slice number.
- cfg Pointer to bit slice configuration.

# **Return values**

None. -

static inline uint32\_t PINT\_PatternMatchGetStatus(PINT\_Type \*base, pint\_pmatch\_bslice\_t bslice)

Get pattern match bit slice status.

This function returns the status of selected bit slice.

# **Parameters**

- base Base address of the PINT peripheral.
- bslice Pattern match bit slice number.

#### **Return values**

status – = 0 Match has not been detected. = 1 Match has been detected.

static inline uint32\_t PINT PatternMatchGetStatusAll(PINT\_Type \*base)

Get status of all pattern match bit slices.

This function returns the status of all bit slices.

#### **Parameters**

• base – Base address of the PINT peripheral.

#### **Return values**

status – Each bit position indicates the match status of corresponding bit slice.

= 0 Match has not been detected. = 1 Match has been detected.

uint32\_t PINT PatternMatchResetDetectLogic(PINT\_Type \*base)

Reset pattern match detection logic.

This function resets the pattern match detection logic if any of the product term is matching.

#### **Parameters**

• base – Base address of the PINT peripheral.

#### **Return values**

pmstatus – Each bit position indicates the match status of corresponding bit slice. = 0 Match was detected. = 1 Match was not detected.

static inline void PINT\_PatternMatchEnable(PINT\_Type \*base)

Enable pattern match function.

This function enables the pattern match function.

#### **Parameters**

• base – Base address of the PINT peripheral.

#### **Return values**

None. -

static inline void PINT\_PatternMatchDisable(PINT\_Type \*base)

Disable pattern match function.

This function disables the pattern match function.

#### **Parameters**

• base – Base address of the PINT peripheral.

# Return values

None. -

static inline void PINT PatternMatchEnableRXEV(PINT Type \*base)

Enable RXEV output.

This function enables the pattern match RXEV output.

# **Parameters**

• base – Base address of the PINT peripheral.

#### **Return values**

None. -

 $static\ in line\ void\ \mathrm{PINT\_PatternMatchDisableRXEV}(PINT\_Type\ *base)$ 

Disable RXEV output.

This function disables the pattern match RXEV output.

## **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

None. -

 $void\ \mathrm{PINT\_EnableCallback}(PINT\_Type\ *base)$ 

Enable callback.

This function enables the interrupt for the selected PINT peripheral. Although the pin(s) are monitored as soon as they are enabled, the callback function is not enabled until this function is called.

#### **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

None. -

void PINT \_DisableCallback(PINT\_Type \*base)

Disable callback.

This function disables the interrupt for the selected PINT peripheral. Although the pins are still being monitored but the callback function is not called.

#### **Parameters**

• base – Base address of the peripheral.

# **Return values**

None. -

void PINT\_Deinit(PINT\_Type \*base)

Deinitialize PINT peripheral.

This function disables the PINT clock.

## **Parameters**

• base – Base address of the PINT peripheral.

# **Return values**

None. -

void PINT\_EnableCallbackByIndex(PINT\_Type \*base, pint\_pin\_int\_t pintIdx) enable callback by pin index.

This function enables callback by pin index instead of enabling all pins.

## **Parameters**

- base Base address of the peripheral.
- pintIdx pin index.

# **Return values**

None. -

void PINT\_DisableCallbackByIndex(PINT\_Type \*base, pint\_pin\_int\_t pintIdx)

disable callback by pin index.

This function disables callback by pin index instead of disabling all pins.

# **Parameters**

- base Base address of the peripheral.
- pintIdx pin index.

# **Return values**

None. -

```
PINT_USE_LEGACY_CALLBACK
PININT_BITSLICE_SRC_START
PININT_BITSLICE_SRC_MASK
PININT_BITSLICE_CFG_START
PININT_BITSLICE_CFG_MASK
PININT_BITSLICE_ENDP_MASK
PINT_PIN_INT_LEVEL
PINT_PIN_INT_EDGE
PINT_PIN_INT_FALL_OR_HIGH_LEVEL
PINT_PIN_INT_RISE
PINT_PIN_RISE_EDGE
PINT_PIN_FALL_EDGE
PINT_PIN_BOTH_EDGE
PINT_PIN_LOW_LEVEL
PINT_PIN_HIGH_LEVEL
struct __pint__status
    #include <fsl_pint.h> PINT event status.
struct _pint_pmatch_cfg
    #include <fsl_pint.h>
```

# 2.16 Power Driver

```
enum pd_bits

Values:

enumerator kPDRUNCFG_PD_FRO_OUT

enumerator kPDRUNCFG_PD_FRO

enumerator kPDRUNCFG_PD_FLASH

enumerator kPDRUNCFG_PD_BOD

enumerator kPDRUNCFG_PD_ADCO

enumerator kPDRUNCFG_PD_LPOSC

enumerator kPDRUNCFG_PD_ACMP

enumerator kPDRUNCFG_ForceUnsigned

enum __power_wakeup

Deep sleep and power down mode wake up configurations.

Values:
```

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```
enumerator kPDAWAKECFG_Wakeup_FRO_OUT
    enumerator kPDAWAKECFG_Wakeup_FRO
    enumerator kPDAWAKECFG Wakeup FLASH
    enumerator kPDAWAKECFG_Wakeup_BOD
    enumerator kPDAWAKECFG_Wakeup_ADC
    enumerator kPDAWAKECFG Wakeup LPOSC
    enumerator kPDAWAKECFG_Wakeup_ACMP
enum \_power\_dpd\_wakeup\_pin
    Deep power down mode wake up pins.
    Values:
    enumerator kPmu_Dpd_En_Pio0_15
    enumerator kPmu_Dpd_En_Pio0_9
    enumerator kPmu Dpd En Pio0 8
    enumerator kPmu Dpd En Pio0 17
    enumerator kPmu_Dpd_En_Pio0_13
    enumerator kPmu Dpd En Pio0 4
    enumerator kPmu_Dpd_En_Pio0_11
    enumerator kPmu_Dpd_En_Pio0_10
enum _power_deep_sleep_active
    Deep sleep/power down mode active part.
    Values:
    enumerator kPDSLEEPCFG DeepSleepBODActive
    enumerator kPDSLEEPCFG DeepSleepLPOscActive
enum _power_gen_reg
    pmu general purpose register index
    Values:
    enumerator kPmu_GenReg0
        general purpose register0
    enumerator kPmu_GenReg1
        general purpose register1
    enumerator kPmu GenReg2
        general purpose register2
    enumerator kPmu_GenReg3
        general purpose register3
    enumerator kPmu GenReg4
        general purpose reguster4
enum _power_mode_config
    Values:
```

```
enumerator kPmu Sleep
     enumerator kPmu_Deep_Sleep
     enumerator kPmu PowerDown
    enumerator kPmu_Deep_PowerDown
enum power bod reset level
    BOD reset level, if VDD below reset level value, the reset will be asserted.
     Values:
     enumerator kBod ResetLevel0
         BOD Reset Level0: 1.51V.
enum _power_bod_interrupt_level
    BOD interrupt level, if VDD below interrupt level value, the BOD interrupt will be asserted.
     Values:
     enumerator kBod InterruptLevelReserved
         BOD interrupt level reserved.
     enumerator kBod_InterruptLevel1
         BOD interrupt level1: 2.24V.
    enumerator kBod_InterruptLevel2
         BOD interrupt level2: 2.52V.
     enumerator kBod InterruptLevel3
         BOD interrupt level3: 2.81V.
typedef enum pd_bits pd_bit_t
typedef enum _power_gen_reg power_gen_reg_t
    pmu general purpose register index
typedef enum _power_mode_config power mode cfg t
typedef enum _power_bod_reset_level power_bod_reset_level_t
    BOD reset level, if VDD below reset level value, the reset will be asserted.
typedef enum _power_bod_interrupt_level power_bod_interrupt_level t
    BOD interrupt level, if VDD below interrupt level value, the BOD interrupt will be asserted.
FSL POWER DRIVER VERSION
    power driver version 2.1.0.
PMUC PCON RESERVED MASK
    PMU PCON reserved mask, used to clear reserved field which should not write 1.
POWER EnbaleLPO
static inline void POWER_EnablePD(pd_bit_t en)
     API to enable PDRUNCFG bit in the Syscon. Note that enabling the bit powers down the
    peripheral.
         Parameters
              • en – peripheral for which to enable the PDRUNCFG bit
         Returns
```

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none

static inline void POWER\_DisablePD( $pd\_bit\_t$  en)

API to disable PDRUNCFG bit in the Syscon. Note that disabling the bit powers up the peripheral.

#### **Parameters**

• en – peripheral for which to disable the PDRUNCFG bit

#### **Returns**

none

static inline void POWER\_EnableLPO(bool enable)

API to enable LPO.

## **Parameters**

• enable – true to enable LPO, false to disable LPO.

static inline void POWER\_WakeUpConfig(uint32\_t mask, bool powerDown)

API to config wakeup configurations for deep sleep mode and power down mode.

#### **Parameters**

- mask wake up configurations for deep sleep mode and power down mode, reference \_power\_wakeup.
- powerDown true is power down the mask part, false is powered part.

static inline void POWER\_DeepSleepConfig(uint32\_t mask, bool powerDown)

API to config active part for deep sleep mode and power down mode.

#### **Parameters**

- mask active part configurations for deep sleep mode and power down mode, reference \_power\_deep\_sleep\_active.
- powerDown true is power down the mask part, false is powered part.

 $static\ in line\ void\ {\rm POWER\_EnableDeepSleep}(void)$ 

API to enable deep sleep bit in the ARM Core.

#### Returns

none

 $static\ in line\ void\ \mathrm{POWER\_DisableDeepSleep}(void)$ 

API to disable deep sleep bit in the ARM Core.

#### Returns

none

void POWER EnterSleep(void)

API to enter sleep power mode.

### Returns

none

void POWER\_EnterDeepSleep(uint32\_t activePart)

API to enter deep sleep power mode.

# **Parameters**

 activePart – should be a single or combine value of \_power\_deep\_sleep\_active.

#### **Returns**

none

void POWER EnterPowerDown(uint32\_t activePart)

API to enter power down mode.

#### **Parameters**

 activePart – should be a single or combine value of \_power\_deep\_sleep\_active.

#### **Returns**

none

 $void\ \mathrm{POWER\_EnterDeepPowerDownMode}(void)$ 

API to enter deep power down mode.

#### **Returns**

none

static inline uint32\_t POWER GetSleepModeFlag(void)

API to get sleep mode flag.

#### **Returns**

sleep mode flag: 0 is active mode, 1 is sleep mode entered.

static inline void POWER ClrSleepModeFlag(void)

API to clear sleep mode flag.

static inline uint32\_t POWER GetDeepPowerDownModeFlag(void)

API to get deep power down mode flag.

#### **Returns**

sleep mode flag: 0 not deep power down, 1 is deep power down mode entered.

 $static\ in line\ void\ {\rm POWER\_ClrDeepPowerDownModeFlag}(void)$ 

API to clear deep power down mode flag.

 $static\ in line\ void\ {\rm POWER\_ClrWakeupPinFlag}(void)$ 

API to clear wake up pin status flag.

static inline void POWER\_DeepPowerDownWakeupSourceSelect(uint32\_t wakeup\_pin)

static inline void POWER EnableNonDpd(bool enable)

API to enable non deep power down mode.

## **Parameters**

• enable – true is enable non deep power down, otherwise disable.

static inline void POWER\_SetRetainData(power\_gen\_reg\_t index, uint32\_t data)

API to retore data to general purpose register which can be retain during deep power down mode.

#### **Parameters**

- index general purpose data register index.
- data data to restore.

static inline uint32\_t POWER GetRetainData(power\_gen\_reg\_t index)

API to get data from general purpose register which retain during deep power down mode.

# **Parameters**

• index – general purpose data register index.

#### Returns

data stored in the general purpose register.

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static inline void POWER\_SetBodLevel(power\_bod\_reset\_level\_t resetLevel, power\_bod\_interrupt\_level\_t interruptLevel, bool enable)

Set Bod interrupt level and reset level.

# **Parameters**

- resetLevel BOD reset threshold level, please refer to power\_bod\_reset\_level\_t.
- interruptLevel BOD interrupt threshold level, please refer to power\_bod\_interrupt\_level\_t.
- enable Used to enable/disable the BOD interrupt and BOD reset.

# 2.17 Reset Driver

```
enum _SYSCON_ RSTn
```

Enumeration for peripheral reset control bits.

Defines the enumeration for peripheral reset control bits in PRESETC-TRL/ASYNCPRESETCTRL registers

Values:

 $enumerator \ \mathrm{kFLASH\_RST\_N\_SHIFT\_RSTn}$ 

Flash controller reset control

enumerator  $kI2C0\_RST\_N\_SHIFT\_RSTn$ 

I2C0 reset control

 $enumerator \ kGPIO0\_RST\_N\_SHIFT\_RSTn$ 

GPIO0 reset control

 $enumerator \ kSWM\_RST\_N\_SHIFT\_RSTn$ 

SWM reset control

 $enumerator \ kWKT\_RST\_N\_SHIFT\_RSTn$ 

Self-wake-up timer(WKT) reset control

enumerator kMRT RST N SHIFT RSTn

Multi-rate timer(MRT) reset control

 ${\bf enumerator~kSPI0\_RST\_N\_SHIFT\_RSTn}$ 

SPI0 reset control.

enumerator kCRC\_RST\_SHIFT\_RSTn

CRC reset control

enumerator  $kUART0\_RST\_N\_SHIFT\_RSTn$ 

UART0 reset control

enumerator kUART1\_RST\_N\_SHIFT\_RSTn

**UART1** reset control

 $enumerator \ {\rm kIOCON\_RST\_N\_SHIFT\_RSTn}$ 

**IOCON** reset control

enumerator kACMP RST N SHIFT RSTn

Analog comparator reset control

 $enumerator~kADC\_RST\_N\_SHIFT\_RSTn$ 

ADC reset control

 $enumerator \ kCTIMER0\_RST\_N\_SHIFT\_RSTn$ 

CTIMER0 reset control

 $enumerator \ kGPIOINT\_RST\_N\_SHIFT\_RSTn$ 

**GPIOINT** reset control

enumerator kFRG0 RST N SHIFT RSTn

Fractional baud rate generator 0 reset control

enumerator kOTHER RST N SHIFT RSTn

Some functions don't need reset

typedef enum \_SYSCON\_RSTn SYSCON\_RSTn\_t

Enumeration for peripheral reset control bits.

Defines the enumeration for peripheral reset control bits in PRESETC-TRL/ASYNCPRESETCTRL registers

typedef SYSCON\_RSTn\_t reset\_ip\_name\_t

 $void \ {\tt RESET\_SetPeripheralReset}(\textit{reset\_ip\_name\_t} \ peripheral)$ 

Assert reset to peripheral.

Asserts reset signal to specified peripheral module.

#### **Parameters**

• peripheral – Assert reset to this peripheral. The enum argument contains encoding of reset register and reset bit position in the reset register.

void RESET\_ClearPeripheralReset(reset\_ip\_name\_t peripheral)

Clear reset to peripheral.

Clears reset signal to specified peripheral module, allows it to operate.

# **Parameters**

• peripheral – Clear reset to this peripheral. The enum argument contains encoding of reset register and reset bit position in the reset register.

void RESET PeripheralReset(reset\_ip\_name\_t peripheral)

Reset peripheral module.

Reset peripheral module.

# **Parameters**

• peripheral – Peripheral to reset. The enum argument contains encoding of reset register and reset bit position in the reset register.

static inline void RESET ReleasePeripheralReset(reset ip name t peripheral)

Release peripheral module.

Release peripheral module.

# **Parameters**

• peripheral – Peripheral to release. The enum argument contains encoding of reset register and reset bit position in the reset register.

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```
FLASH RSTS N
    Array initializers with peripheral reset bits
I2C_RSTS_N
GPIO_RSTS_N
SWM_RSTS_N
WKT_RSTS_N
MRT_RSTS_N
SPI RSTS N
CRC RSTS N
UART RSTS N
IOCON_RSTS_N
ACMP_RSTS_N
ADC_RSTS_N
CTIMER_RSTS_N
GPIOINT_RSTS_N
FRG_RSTS_N
WWDT_RSTS_N
```

# 2.18 SPI: Serial Peripheral Interface Driver

# 2.19 SPI Driver

void SPI\_MasterGetDefaultConfig(spi\_master\_config\_t \*config)

Sets the SPI master configuration structure to default values.

The purpose of this API is to get the configuration structure initialized for use in SPI\_MasterInit(). User may use the initialized structure unchanged in SPI\_MasterInit(), or modify some fields of the structure before calling SPI\_MasterInit(). After calling this API, the master is ready to transfer. Example:

```
spi_master_config_t config;
SPI_MasterGetDefaultConfig(&config);
```

#### **Parameters**

• config – pointer to master config structure

 $status\_t \ \mathrm{SPI\_MasterInit}(SPI\_Type *base, const \ spi\_master\_config\_t *config, uint32\_t \ srcClock\_Hz)$  Initializes the SPI with master configuration.

The configuration structure can be filled by user from scratch, or be set with default values by SPI\_MasterGetDefaultConfig(). After calling this API, the slave is ready to transfer. Example

```
spi_master_config_t config = {
    .baudRate_Bps = 500000,
    ...
};
SPI_MasterInit(SPI0, &config);
```

## **Parameters**

- base SPI base pointer
- config pointer to master configuration structure
- srcClock Hz Source clock frequency.

void SPI\_SlaveGetDefaultConfig(spi\_slave\_config\_t \*config)

Sets the SPI slave configuration structure to default values.

The purpose of this API is to get the configuration structure initialized for use in SPI\_SlaveInit(). Modify some fields of the structure before calling SPI\_SlaveInit(). Example:

```
spi_slave_config_t config;
SPI_SlaveGetDefaultConfig(&config);
```

#### **Parameters**

• config – pointer to slave configuration structure

 $status\_t \ \mathrm{SPI\_SlaveInit}(SPI\_Type \ *base, \ const \ spi\_slave\_config\_t \ *config)$ 

Initializes the SPI with slave configuration.

The configuration structure can be filled by user from scratch or be set with default values by SPI\_SlaveGetDefaultConfig(). After calling this API, the slave is ready to transfer. Example

```
spi_slave_config_t config = {
.polarity = kSPI_ClockPolarityActiveHigh;
.phase = kSPI_ClockPhaseFirstEdge;
.direction = kSPI_MsbFirst;
...
};
SPI_SlaveInit(SPI0, &config);
```

# **Parameters**

- base SPI base pointer
- config pointer to slave configuration structure

void SPI Deinit(SPI Type \*base)

De-initializes the SPI.

Calling this API resets the SPI module, gates the SPI clock. Disable the fifo if enabled. The SPI module can't work unless calling the SPI\_MasterInit/SPI\_SlaveInit to initialize module.

#### **Parameters**

• base – SPI base pointer

static inline void SPI Enable(SPI Type \*base, bool enable)

Enable or disable the SPI Master or Slave.

# **Parameters**

• base – SPI base pointer

• enable – or disable (true = enable, false = disable)

static inline uint32\_t SPI GetStatusFlags(SPI\_Type \*base)

Gets the status flag.

# **Parameters**

• base – SPI base pointer

## **Returns**

SPI Status, use status flag to AND \_spi\_status\_flags could get the related status.

 $static\ in line\ void\ {\rm SPI\_ClearStatusFlags}(SPI\_Type\ *base,\ uint 32\_t\ mask)$ 

Clear the status flag.

#### **Parameters**

- base SPI base pointer
- mask SPI Status, use status flag to AND \_spi\_status\_flags could get the related status.

static inline void SPI\_EnableInterrupts(SPI\_Type \*base, uint32\_t irqs)

Enables the interrupt for the SPI.

#### **Parameters**

- base SPI base pointer
- $\bullet$  irqs SPI interrupt source. The parameter can be any combination of the following values:
  - kSPI\_RxReadyInterruptEnable
  - kSPI\_TxReadyInterruptEnable

static inline void SPI\_DisableInterrupts(SPI\_Type \*base, uint32\_t irqs)

Disables the interrupt for the SPI.

# **Parameters**

- base SPI base pointer
- ${\rm irqs}$  SPI interrupt source. The parameter can be any combination of the following values:
  - kSPI\_RxReadyInterruptEnable
  - kSPI\_TxReadyInterruptEnable

static inline bool SPI\_IsMaster(SPI\_Type \*base)

Returns whether the SPI module is in master mode.

# **Parameters**

• base – SPI peripheral address.

## **Returns**

Returns true if the module is in master mode or false if the module is in slave mode.

 $status\_t \ \mathrm{SPI\_MasterSetBaudRate}(SPI\_Type \ *base, uint 32\_t \ baudrate\_Bps, uint 32\_t \ srcClock\_Hz)$  Sets the baud rate for SPI transfer. This is only used in master.

#### **Parameters**

- base SPI base pointer
- baudrate Bps baud rate needed in Hz.
- srcClock\_Hz SPI source clock frequency in Hz.

static inline void SPI WriteData(SPI\_Type \*base, uint16\_t data)

Writes a data into the SPI data register directly.

#### **Parameters**

- base SPI base pointer
- data needs to be write.

static inline void SPI\_WriteConfigFlags(SPI\_Type \*base, uint32\_t configFlags)

Writes a data into the SPI TXCTL register directly.

#### **Parameters**

- base SPI base pointer
- configFlags control command needs to be written.

void SPI\_WriteDataWithConfigFlags(SPI\_Type \*base, uint16\_t data, uint32\_t configFlags)

Writes a data control info and data into the SPI TX register directly.

#### **Parameters**

- base SPI base pointer
- data value needs to be written.
- configFlags control command needs to be written.

static inline uint32 t SPI ReadData(SPI Type \*base)

Gets a data from the SPI data register.

#### **Parameters**

• base – SPI base pointer

#### **Returns**

Data in the register.

void SPI SetTransferDelay(SPI\_Type \*base, const spi\_delay\_config\_t \*config)

Set delay time for transfer. the delay uint is SPI clock time, maximum value is 0xF.

#### **Parameters**

- base SPI base pointer
- config configuration for delay option spi\_delay\_config\_t.

void SPI\_SetDummyData(SPI\_Type \*base, uint16\_t dummyData)

Set up the dummy data. This API can change the default data to be transferred when users set the tx buffer to NULL.

#### **Parameters**

- base SPI peripheral address.
- dummyData Data to be transferred when tx buffer is NULL.

status\_t SPI\_MasterTransferBlocking(SPI\_Type \*base, spi\_transfer\_t \*xfer)

Transfers a block of data using a polling method.

# **Parameters**

- base SPI base pointer
- xfer pointer to spi\_xfer\_config\_t structure

# **Return values**

- kStatus\_Success Successfully start a transfer.
- kStatus InvalidArgument Input argument is invalid.

• kStatus SPI Timeout – The transfer timed out and was aborted.

status\_t SPI\_MasterTransferCreateHandle(SPI\_Type \*base, spi\_master\_handle\_t \*handle, spi\_master\_callback\_t callback, void \*userData)

Initializes the SPI master handle.

This function initializes the SPI master handle which can be used for other SPI master transactional APIs. Usually, for a specified SPI instance, call this API once to get the initialized handle.

#### **Parameters**

- base SPI peripheral base address.
- handle SPI handle pointer.
- callback Callback function.
- userData User data.

status\_t SPI\_MasterTransferNonBlocking(SPI\_Type \*base, spi\_master\_handle\_t \*handle, spi\_transfer\_t \*xfer)

Performs a non-blocking SPI interrupt transfer.

#### **Parameters**

- base SPI peripheral base address.
- handle pointer to spi\_master\_handle\_t structure which stores the transfer state
- xfer pointer to spi xfer config t structure

#### **Return values**

- kStatus\_Success Successfully start a transfer.
- kStatus InvalidArgument Input argument is invalid.
- kStatus SPI Busy SPI is not idle, is running another transfer.

Gets the master transfer count.

This function gets the master transfer count.

#### **Parameters**

- base SPI peripheral base address.
- handle Pointer to the spi\_master\_handle\_t structure which stores the transfer state.
- count The number of bytes transferred by using the non-blocking transaction.

#### Returns

status of status\_t.

 $void \ \mathrm{SPI\_MasterTransferAbort}(SPI\_Type \ *base, \textit{spi\_master\_handle\_t} \ *handle)$ 

SPI master aborts a transfer using an interrupt.

This function aborts a transfer using an interrupt.

# **Parameters**

- base SPI peripheral base address.
- handle Pointer to the spi\_master\_handle\_t structure which stores the transfer state.

void SPI\_MasterTransferHandleIRQ(SPI\_Type \*base, spi\_master\_handle\_t \*handle) Interrupts the handler for the SPI.

#### **Parameters**

- base SPI peripheral base address.
- handle pointer to spi\_master\_handle\_t structure which stores the transfer state.

status\_t SPI\_SlaveTransferCreateHandle(SPI\_Type \*base, spi\_slave\_handle\_t \*handle, spi\_slave\_callback\_t callback, void \*userData)

Initializes the SPI slave handle.

This function initializes the SPI slave handle which can be used for other SPI slave transactional APIs. Usually, for a specified SPI instance, call this API once to get the initialized handle.

#### **Parameters**

- base SPI peripheral base address.
- handle SPI handle pointer.
- callback Callback function.
- userData User data.

status\_t SPI\_SlaveTransferNonBlocking(SPI\_Type \*base, spi\_slave\_handle\_t \*handle, spi\_transfer\_t \*xfer)

Performs a non-blocking SPI slave interrupt transfer.

**Note:** The API returns immediately after the transfer initialization is finished.

## **Parameters**

- base SPI peripheral base address.
- handle pointer to spi\_master\_handle\_t structure which stores the transfer state
- xfer pointer to spi xfer config t structure

# **Return values**

- kStatus Success Successfully start a transfer.
- kStatus\_InvalidArgument Input argument is invalid.
- kStatus SPI Busy SPI is not idle, is running another transfer.

static inline *status\_t* SPI\_SlaveTransferGetCount(SPI\_Type \*base, *spi\_slave\_handle\_t* \*handle, size\_t \*count)

Gets the slave transfer count.

This function gets the slave transfer count.

# **Parameters**

- base SPI peripheral base address.
- handle Pointer to the spi\_master\_handle\_t structure which stores the transfer state.
- $\bullet \ {\rm count}$  The number of bytes transferred by using the non-blocking transaction.

#### **Returns**

status of status\_t.

static inline void SPI\_SlaveTransferAbort(SPI\_Type \*base, spi\_slave\_handle\_t \*handle)

SPI slave aborts a transfer using an interrupt.

This function aborts a transfer using an interrupt.

#### **Parameters**

- base SPI peripheral base address.
- handle Pointer to the spi\_slave\_handle\_t structure which stores the transfer state.

void SPI\_SlaveTransferHandleIRQ(SPI\_Type \*base, spi\_slave\_handle\_t \*handle)

Interrupts a handler for the SPI slave.

# **Parameters**

- base SPI peripheral base address.
- handle pointer to spi\_slave\_handle\_t structure which stores the transfer state

FSL SPI DRIVER VERSION

SPI driver version.

enum spi xfer option

SPI transfer option.

Values:

enumerator kSPI EndOfFrame

Add delay at the end of each frame(the last clk edge).

enumerator kSPI\_EndOfTransfer

Re-assert the CS signal after transfer finishes to deselect slave.

enumerator kSPI\_ReceiveIgnore

Ignore the receive data.

enum \_spi\_shift\_direction

SPI data shifter direction options.

Values:

enumerator kSPI MsbFirst

Data transfers start with most significant bit.

enumerator kSPI LsbFirst

Data transfers start with least significant bit.

enum spi clock polarity

SPI clock polarity configuration.

Values:

 $enumerator \ kSPI\_ClockPolarityActiveHigh$ 

Active-high SPI clock (idles low).

enumerator kSPI ClockPolarityActiveLow

Active-low SPI clock (idles high).

```
enum _spi_clock_phase
     SPI clock phase configuration.
     Values:
     enumerator kSPI ClockPhaseFirstEdge
         First edge on SCK occurs at the middle of the first cycle of a data transfer.
     enumerator kSPI ClockPhaseSecondEdge
         First edge on SCK occurs at the start of the first cycle of a data transfer.
enum _spi_ssel
     Slave select.
     Values:
     enumerator~\mathrm{kSPI\_Ssel0Assert}
         Slave select 0
     enumerator kSPI_SselDeAssertAll
enum _spi_spol
     ssel polarity
     Values:
     enumerator kSPI_Spol0ActiveHigh
     enumerator kSPI_Spol1ActiveHigh
     enumerator kSPI_Spol2ActiveHigh
     enumerator kSPI_Spol3ActiveHigh
     enumerator \ kSPI\_SpolActiveAllHigh
     enumerator kSPI SpolActiveAllLow
enum spi data width
     Transfer data width.
     Values:
     enumerator kSPI Data4Bits
         4 bits data width
     enumerator kSPI_Data5Bits
         5 bits data width
     enumerator kSPI Data6Bits
         6 bits data width
     enumerator kSPI Data7Bits
         7 bits data width
     enumerator kSPI Data8Bits
         8 bits data width
     enumerator kSPI Data9Bits
         9 bits data width
     enumerator kSPI Data10Bits
         10 bits data width
```

```
enumerator kSPI_Data11Bits
         11 bits data width
     enumerator kSPI Data12Bits
         12 bits data width
     enumerator kSPI Data13Bits
         13 bits data width
     enumerator kSPI Data14Bits
         14 bits data width
     enumerator kSPI Data15Bits
         15 bits data width
     enumerator kSPI Data16Bits
         16 bits data width
     SPI transfer status.
     Values:
     enumerator kStatus_SPI_Busy
         SPI bus is busy
     enumerator kStatus SPI Idle
         SPI is idle
     enumerator kStatus SPI Error
         SPI error
     enumerator kStatus_SPI_BaudrateNotSupport
         Baudrate is not support in current clock source
     enumerator kStatus_SPI_Timeout
         SPI Timeout polling status flags.
enum spi interrupt enable
     SPI interrupt sources.
     Values:
     enumerator kSPI RxReadyInterruptEnable
         Rx ready interrupt
     enumerator kSPI TxReadyInterruptEnable
         Tx ready interrupt
     enumerator kSPI RxOverrunInterruptEnable
         Rx overrun interrupt
     {\bf enumerator} \ {\rm kSPI\_TxUnderrunInterruptEnable}
         Tx underrun interrupt
     enumerator kSPI SlaveSelectAssertInterruptEnable
         Slave select assert interrupt
     enumerator kSPI SlaveSelectDeassertInterruptEnable
         Slave select deassert interrupt
     enumerator kSPI AllInterruptEnable
```

```
enum _spi_status_flags
     SPI status flags.
     Values:
     enumerator kSPI RxReadyFlag
          Receive ready flag.
     enumerator kSPI TxReadyFlag
          Transmit ready flag.
     enumerator kSPI RxOverrunFlag
          Receive overrun flag.
     enumerator kSPI TxUnderrunFlag
          Transmit underrun flag.
     enumerator kSPI SlaveSelectAssertFlag
          Slave select assert flag.
     enumerator kSPI SlaveSelectDeassertFlag
          slave select deassert flag.
     enumerator kSPI_StallFlag
          Stall flag.
     enumerator kSPI EndTransferFlag
          End transfer bit.
     enumerator kSPI MasterIdleFlag
          Master in idle status flag.
typedef enum _spi_shift_direction spi_shift_direction_t
     SPI data shifter direction options.
typedef enum _spi_clock_polarity spi_clock_polarity_t
     SPI clock polarity configuration.
typedef enum _spi_clock_phase spi_clock_phase_t
     SPI clock phase configuration.
typedef\ enum\ \_spi\_ssel\ \mathrm{spi}\_\mathrm{ssel}\_\mathrm{t}
     Slave select.
typedef enum _spi_spol spi_spol_t
     ssel polarity
typedef enum _spi_data_width spi_data_width_t
     Transfer data width.
typedef\ struct\_spi\_delay\_config\ \mathrm{spi\_delay\_config\_t}
     SPI delay time configure structure.
typedef struct _spi_master_config spi_master_config_t
     SPI master user configure structure.
typedef struct _spi_slave_config spi_slave_config_t
     SPI slave user configure structure.
typedef\ struct\_spi\_transfer\ spi\_transfer\_t
     SPI transfer structure.
```

```
typedef struct _spi_master_handle spi_master_handle_t
     Master handle type.
typedef spi_master_handle_t spi_slave_handle_t
     Slave handle type.
typedef void (*spi_master_callback_t)(SPI_Type *base, spi_master_handle_t *handle, status_t
status, void *userData)
     SPI master callback for finished transmit.
typedef void (*spi_slave_callback_t)(SPI_Type *base, spi_slave_handle_t *handle, status_t status,
void *userData)
     SPI slave callback for finished transmit.
volatile uint16_t s dummyData[]
uint32_t SPI_GetInstance(SPI_Type *base)
     Returns instance number for SPI peripheral base address.
SPI DUMMYDATA
     SPI dummy transfer data, the data is sent while txBuff is NULL.
FSL_SDK_ENABLE_SPI_DRIVER_TRANSACTIONAL_APIS
SPI_RETRY_TIMES
     Retry times for waiting flag.
struct _spi_delay_config
     #include <fsl spi.h> SPI delay time configure structure.
     Public Members
     uint8_t preDelay
         Delay between SSEL assertion and the beginning of transfer.
     uint8_t postDelay
         Delay between the end of transfer and SSEL deassertion.
     uint8 t frameDelay
         Delay between frame to frame.
     uint8_t transferDelay
         Delay between transfer to transfer.
struct spi master config
     #include <fsl_spi.h> SPI master user configure structure.
     Public Members
     bool enableLoopback
         Enable loopback for test purpose
     bool enableMaster
         Enable SPI at initialization time
     uint32_t baudRate Bps
         Baud Rate for SPI in Hz
     spi_clock_polarity_t clockPolarity
         Clock polarity
```

```
spi\_clock\_phase\_t clockPhase
          Clock phase
     spi_shift_direction_t direction
          MSB or LSB
     uint8 t dataWidth
          Width of the data
     spi\_ssel\_t sselNumber
          Slave select number
     spi_spol_t sselPolarity
          Configure active CS polarity
     spi\_delay\_config\_t  delayConfig
          Configure for delay time.
struct _spi_slave_config
     #include <fsl_spi.h> SPI slave user configure structure.
     Public Members
     bool enableSlave
          Enable SPI at initialization time
     spi\_clock\_polarity\_t \ {\it clockPolarity}
          Clock polarity
     spi\_clock\_phase\_t \ {\it clockPhase}
          Clock phase
     spi_shift_direction_t direction
          MSB or LSB
     uint8 t dataWidth
          Width of the data
     spi\_spol\_t sselPolarity
          Configure active CS polarity
struct \_spi\_transfer
     #include <fsl_spi.h> SPI transfer structure.
     Public Members
     const uint8 t*txData
          Send buffer
     uint8 t*rxData
          Receive buffer
     size_t dataSize
          Transfer bytes
     uint 32\_t \ {\rm configFlags}
          Additional option to control transfer _spi_xfer_option.
struct \_spi\_master\_handle
```

#include <fsl\_spi.h> SPI transfer handle structure.

# **Public Members**

```
const uint8 t *volatile txData
    Transfer buffer
uint8 t *volatile rxData
    Receive buffer
volatile\ size\_t\ \mathrm{txRemainingBytes}
    Number of data to be transmitted [in bytes]
volatile size_t rxRemainingBytes
    Number of data to be received [in bytes]
size_t totalByteCount
    A number of transfer bytes
volatile uint32_t state
    SPI internal state
spi\_master\_callback\_t callback
    SPI callback
void *userData
    Callback parameter
uint8 t dataWidth
    Width of the data [Valid values: 1 to 16]
uint32\_t lastCommand
    Last command for transfer.
```

# 2.20 SWM: Switch Matrix Module

```
enum _swm_port_pin_type_t
    SWM port_pin number.
    Values:
    enumerator kSWM PortPin P0 0
        port_pin number P0_0.
    enumerator kSWM PortPin P0 1
        port_pin number P0_1.
    enumerator kSWM_PortPin_P0_2
        port_pin number P0_2.
    enumerator kSWM PortPin P0 3
        port_pin number P0_3.
    enumerator kSWM PortPin P0 4
        port_pin number P0_4.
    enumerator kSWM PortPin P0 5
        port_pin number P0_5.
    enumerator kSWM_PortPin_P0_6
        port_pin number P0_6.
```

- enumerator kSWM\_PortPin\_P0\_7 port\_pin number P0\_7.
- enumerator kSWM\_PortPin\_P0\_8 port\_pin number P0\_8.
- enumerator kSWM\_PortPin\_P0\_9 port pin number P0 9.
- enumerator kSWM\_PortPin\_P0\_10 port\_pin number P0\_10.
- enumerator kSWM\_PortPin\_P0\_11 port\_pin number P0\_11.
- enumerator kSWM\_PortPin\_P0\_12 port\_pin number P0\_12.
- enumerator kSWM\_PortPin\_P0\_13 port\_pin number P0\_13.
- enumerator kSWM\_PortPin\_P0\_14 port\_pin number P0\_14.
- enumerator kSWM\_PortPin\_P0\_15 port\_pin number P0\_15.
- enumerator kSWM\_PortPin\_P0\_16 port\_pin number P0\_16.
- enumerator kSWM\_PortPin\_P0\_17 port\_pin number P0\_17.
- enumerator kSWM\_PortPin\_Reset port\_pin reset number.
- $enum \_swm\_select\_movable\_t$

SWM movable selection.

# Values:

- $\label{eq:continuity} \begin{array}{c} enumerator \ \mathrm{kSWM\_USART0\_TXD} \\ \\ Movable \ function \ as \ USART0\_TXD. \end{array}$
- $\label{eq:continuous} \begin{array}{c} \text{enumerator kSWM\_USART0\_RXD} \\ \text{Movable function as USART0\_RXD.} \end{array}$
- $\begin{array}{c} enumerator~kSWM\_USART0\_RTS\\ Movable~function~as~USART0\_RTS. \end{array}$
- $\begin{array}{c} enumerator~\mathrm{kSWM\_USART0\_CTS}\\ Movable~function~as~USART0\_CTS. \end{array}$
- enumerator kSWM\_USART0\_SCLK
  Movable function as USART0\_SCLK.
- $\begin{array}{c} enumerator~kSWM\_USART1\_TXD\\ Movable~function~as~USART1\_TXD. \end{array}$
- $\begin{array}{c} \textbf{enumerator} \ kSWM\_USART1\_RXD\\ \textbf{Movable function as} \ \textbf{USART1\_RXD}. \end{array}$

enumerator kSWM\_USART1\_SCLK

Movable function as USART1\_SCLK.

enumerator kSWM\_SPI0\_SCK

Movable function as SPI0\_SCK.

enumerator kSWM\_SPI0\_MOSI

Movable function as SPIO\_MOSI.

enumerator kSWM\_SPI0\_MISO

Movable function as SPI0\_MISO.

enumerator kSWM SPI0 SSEL0

Movable function as SPI0\_SSEL0.

enumerator  $kSWM\_SPI0\_SSEL1$ 

Movable function as SPI0\_SSEL1.

enumerator kSWM\_T0\_CAP\_CHN0

Movable function as Timer Capture Channel 0.

enumerator kSWM\_T0\_CAP\_CHN1

Movable function as Timer Capture Channel 1.

enumerator  $kSWM\_T0\_CAP\_CHN2$ 

Movable function as Timer Capture Channel 2.

enumerator kSWM\_T0\_MAT\_CHN0

Movable function as Timer Match Channel 0.

enumerator kSWM\_T0\_MAT\_CHN1

Movable function as Timer Match Channel 1.

enumerator kSWM\_T0\_MAT\_CHN2

Movable function as Timer Match Channel 2.

enumerator kSWM\_T0\_MAT\_CHN3

Movable function as Timer Match Channel 3.

enumerator kSWM\_I2C0\_SDA

Movable function as I2C1\_SDA.

enumerator kSWM I2C0 SCL

Movable function as I2C1 SCL.

enumerator  $kSWM\_ACMP\_OUT$ 

Movable function as ACMP OUT.

enumerator  $kSWM\_CLKOUT$ 

Movable function as CLKOUT.

enumerator kSWM\_GPIO\_INT\_BMAT

Movable function as GPIO\_INT\_BMAT.

enumerator kSWM\_LVLSHFT\_IN0

Movable function as LVLSHFT\_IN0.

enumerator kSWM LVLSHFT IN1

Movable function as LVLSHFT\_IN1.

enumerator kSWM\_LVLSHFT\_OUT0

Movable function as LVLSHFT\_OUT0.

enumerator kSWM LVLSHFT OUT1

Movable function as LVLSHFT\_OUT1.

enumerator kSWM\_MOVABLE\_NUM\_FUNCS

Movable function number.

enum \_swm\_select\_fixed\_pin\_t

SWM fixed pin selection.

Values:

enumerator  $kSWM\_ACMP\_INPUT1$ 

Fixed-pin function as ACMP\_INPUT1.

enumerator kSWM ACMP INPUT2

Fixed-pin function as ACMP\_INPUT2.

enumerator kSWM ACMP INPUT3

Fixed-pin function as ACMP\_INPUT3.

enumerator  $kSWM\_ACMP\_INPUT4$ 

Fixed-pin function as ACMP\_INPUT4.

enumerator kSWM SWCLK

Fixed-pin function as SWCLK.

enumerator kSWM SWDIO

Fixed-pin function as SWDIO.

enumerator kSWM RESETN

Fixed-pin function as RESETN.

enumerator kSWM CLKIN

Fixed-pin function as CLKIN.

enumerator kSWM WKCLKIN

Fixed-pin function as CLKIN.

enumerator kSWM VDDCMP

Fixed-pin function as VDDCMP.

enumerator  $kSWM\_ADC\_CHN0$ 

Fixed-pin function as ADC\_CHN0.

enumerator kSWM ADC CHN1

Fixed-pin function as ADC\_CHN1.

enumerator kSWM ADC CHN2

Fixed-pin function as ADC\_CHN2.

enumerator kSWM ADC CHN3

Fixed-pin function as ADC\_CHN3.

enumerator kSWM ADC CHN4

Fixed-pin function as ADC\_CHN4.

enumerator kSWM ADC CHN5

Fixed-pin function as ADC\_CHN5.

enumerator kSWM ADC CHN6

Fixed-pin function as ADC\_CHN6.

```
enumerator kSWM ADC CHN7
        Fixed-pin function as ADC_CHN7.
    enumerator kSWM ADC CHN8
        Fixed-pin function as ADC_CHN8.
    enumerator kSWM_ADC_CHN9
        Fixed-pin function as ADC CHN9.
    enumerator kSWM ADC CHN10
        Fixed-pin function as ADC CHN10.
    enumerator kSWM ADC CHN11
        Fixed-pin function as ADC_CHN11.
    enumerator kSWM FIXEDPIN NUM FUNCS
        Fixed-pin function number.
typedef enum _swm_port_pin_type_t swm_port_pin_type_t
    SWM port_pin number.
typedef enum _swm_select_movable_t swm_select_movable_t
    SWM movable selection.
typedef enum _swm_select_fixed_pin_t swm_select_fixed_pin_t
    SWM fixed pin selection.
FSL SWM DRIVER VERSION
    LPC SWM driver version.
void SWM_SetMovablePinSelect(SWM_Type *base, swm_select_movable_t func,
                            swm_port_pin_type_t swm_port_pin)
```

Assignment of digital peripheral functions to pins.

This function will selects a pin (designated by its GPIO port and bit numbers) to a function.

#### **Parameters**

- base SWM peripheral base address.
- func any function name that is movable.
- swm port pin any pin which has a GPIO port number and bit number.

void SWM SetFixedPinSelect(SWM\_Type \*base, swm\_select\_fixed\_pin\_t func, bool enable) Enable the fixed-pin function.

This function will enables a fixed-pin function in PINENABLE0 or PINENABLE1.

# **Parameters**

- base SWM peripheral base address.
- func any function name that is fixed pin.
- enable enable or disable.

#### **SYSCON: System Configuration** 2.21

```
enum syscon connection t
     SYSCON connections type.
     Values:
```

```
enumerator kSYSCON GpioPort0Pin0ToPintsel
         Pin Interrupt.
    enumerator kSYSCON_GpioPort0Pin1ToPintsel
    enumerator kSYSCON_GpioPort0Pin2ToPintsel
    enumerator kSYSCON_GpioPort0Pin3ToPintsel
    enumerator kSYSCON_GpioPort0Pin4ToPintsel
    enumerator kSYSCON_GpioPort0Pin5ToPintsel
    enumerator kSYSCON GpioPort0Pin7ToPintsel
    enumerator kSYSCON GpioPort0Pin8ToPintsel
     enumerator kSYSCON GpioPort0Pin9ToPintsel
    enumerator kSYSCON_GpioPort0Pin10ToPintsel
    enumerator kSYSCON_GpioPort0Pin11ToPintsel
    enumerator kSYSCON_GpioPort0Pin12ToPintsel
    enumerator kSYSCON_GpioPort0Pin13ToPintsel
    {\bf enumerator} \ k SYSCON\_GpioPort0Pin14ToPintsel
    enumerator kSYSCON_GpioPort0Pin15ToPintsel
    enumerator kSYSCON_GpioPort0Pin16ToPintsel
    enumerator kSYSCON_GpioPort0Pin17ToPintsel
typedef enum _syscon_connection_t syscon_connection_t
    SYSCON connections type.
PINTSEL ID
    Periphinmux IDs.
SYSCON SHIFT
FSL SYSON_DRIVER_VERSION
    Group syscon driver version for SDK.
    Version 2.0.1.
```

void SYSCON\_AttachSignal(SYSCON\_Type \*base, uint32\_t index, syscon\_connection\_t connection)

Attaches a signal.

This function gates the SYSCON clock.

# **Parameters**

- base Base address of the SYSCON peripheral.
- index Destination peripheral to attach the signal to.
- connection Selects connection.

#### **Return values**

None. -

# 2.22 USART: Universal Asynchronous Receiver/Transmitter Driver

# 2.23 USART Driver

uint32\_t USART GetInstance(USART\_Type \*base)

Returns instance number for USART peripheral base address.

status\_t USART\_Init(USART\_Type \*base, const usart\_config\_t \*config, uint32\_t srcClock\_Hz)
Initializes a USART instance with user configuration structure and peripheral clock.

This function configures the USART module with the user-defined settings. The user can configure the configuration structure and also get the default configuration by using the USART\_GetDefaultConfig() function. Example below shows how to use this API to configure USART.

```
usart_config_t usartConfig;
usartConfig.baudRate_Bps = 115200U;
usartConfig.parityMode = kUSART_ParityDisabled;
usartConfig.stopBitCount = kUSART_OneStopBit;
USART_Init(USART1, &usartConfig, 200000000U);
```

#### **Parameters**

- base USART peripheral base address.
- config Pointer to user-defined configuration structure.
- srcClock\_Hz USART clock source frequency in HZ.

# **Return values**

- kStatus\_USART\_BaudrateNotSupport Baudrate is not support in current clock source.
- kStatus\_InvalidArgument USART base address is not valid
- kStatus Success Status USART initialize succeed

void USART\_Deinit(USART\_Type \*base)

Deinitializes a USART instance.

This function waits for TX complete, disables the USART clock.

# **Parameters**

• base – USART peripheral base address.

void USART\_GetDefaultConfig(usart\_config\_t \*config)

Gets the default configuration structure.

This function initializes the USART configuration structure to a default value. The default values are: usartConfig->baudRate\_Bps = 9600U; usartConfig->parityMode = kUSART\_ParityDisabled; usartConfig->stopBitCount = kUSART\_OneStopBit; usartConfig->bitCountPerChar = kUSART\_8BitsPerChar; usartConfig->loopback = false; usartConfig->enableTx = false; usartConfig->enableTx = false; usartConfig->enableRx = false; ...

# **Parameters**

• config – Pointer to configuration structure.

status\_t USART\_SetBaudRate(USART\_Type \*base, uint32\_t baudrate\_Bps, uint32\_t srcClock\_Hz)
Sets the USART instance baud rate.

This function configures the USART module baud rate. This function is used to update the USART module baud rate after the USART module is initialized by the USART\_Init.

```
USART_SetBaudRate(USART1, 115200U, 20000000U);
```

#### **Parameters**

- base USART peripheral base address.
- baudrate\_Bps USART baudrate to be set.
- srcClock\_Hz USART clock source frequency in HZ.

# **Return values**

- kStatus\_USART\_BaudrateNotSupport Baudrate is not support in current clock source.
- kStatus\_Success Set baudrate succeed.
- kStatus\_InvalidArgument One or more arguments are invalid.

```
static inline uint32_t USART_GetStatusFlags(USART_Type *base)
```

Get USART status flags.

This function get all USART status flags, the flags are returned as the logical OR value of the enumerators \_usart\_flags. To check a specific status, compare the return value with enumerators in \_usart\_flags. For example, to check whether the RX is ready:

```
if (kUSART_RxReady & USART_GetStatusFlags(USART1)) {
...
}
```

#### **Parameters**

• base – USART peripheral base address.

#### **Returns**

USART status flags which are ORed by the enumerators in the \_usart\_flags.

```
static inline void USART ClearStatusFlags(USART_Type *base, uint32_t mask)
```

Clear USART status flags.

This function clear supported USART status flags For example:

```
USART_ClearStatusFlags(USART1, kUSART_HardwareOverrunFlag)
```

# **Parameters**

- base USART peripheral base address.
- $\operatorname{mask}$  status flags to be cleared.

static inline void USART\_EnableInterrupts(USART\_Type \*base, uint32\_t mask)

Enables USART interrupts according to the provided mask.

This function enables the USART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See \_usart\_interrupt\_enable. For example, to enable TX ready interrupt and RX ready interrupt:

```
 \begin{tabular}{ll} USART\_EnableInterrupts (USART1, kUSART\_RxReadyInterruptEnable \mid kUSART\_\\ \to TxReadyInterruptEnable); \end{tabular}
```

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#### **Parameters**

- base USART peripheral base address.
- mask The interrupts to enable. Logical OR of \_usart\_interrupt\_enable.

static inline void USART\_DisableInterrupts(USART\_Type \*base, uint32\_t mask)

Disables USART interrupts according to a provided mask.

This function disables the USART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See \_usart\_interrupt\_enable. This example shows how to disable the TX ready interrupt and RX ready interrupt:

USART\_DisableInterrupts(USART1, kUSART\_TxReadyInterruptEnable | kUSART\_→RxReadyInterruptEnable);

#### **Parameters**

- base USART peripheral base address.
- mask The interrupts to disable. Logical OR of \_usart\_interrupt\_enable.

static inline uint32\_t USART GetEnabledInterrupts(USART\_Type \*base)

Returns enabled USART interrupts.

This function returns the enabled USART interrupts.

#### **Parameters**

• base – USART peripheral base address.

static inline void USART EnableContinuousSCLK(USART\_Type \*base, bool enable)

Continuous Clock generation. By default, SCLK is only output while data is being transmitted in synchronous mode. Enable this funciton, SCLK will run continuously in synchronous mode, allowing characters to be received on Un\_RxD independently from transmission on Un\_TXD).

# **Parameters**

- base USART peripheral base address.
- enable Enable Continuous Clock generation mode or not, true for enable and false for disable.

static inline void USART\_EnableAutoClearSCLK(USART\_Type \*base, bool enable)

Enable Continuous Clock generation bit auto clear. While enable this cuntion, the Continuous Clock bit is automatically cleared when a complete character has been received. This bit is cleared at the same time.

# **Parameters**

- base USART peripheral base address.
- enable Enable auto clear or not, true for enable and false for disable.

static inline void USART EnableCTS(USART Type \*base, bool enable)

Enable CTS. This function will determine whether CTS is used for flow control.

#### **Parameters**

- base USART peripheral base address.
- enable Enable CTS or not, true for enable and false for disable.

static inline void USART\_EnableTx(USART\_Type \*base, bool enable)

Enable the USART transmit.

This function will enable or disable the USART transmit.

#### **Parameters**

- base USART peripheral base address.
- enable true for enable and false for disable.

static inline void USART EnableRx(USART\_Type \*base, bool enable)

Enable the USART receive.

This function will enable or disable the USART receive. Note: if the transmit is enabled, the receive will not be disabled.

#### **Parameters**

- base USART peripheral base address.
- enable true for enable and false for disable.

static inline void USART WriteByte(USART\_Type \*base, uint8\_t data)

Writes to the TXDAT register.

This function will writes data to the TXDAT automatly. The upper layer must ensure that TXDATA has space for data to write before calling this function.

#### **Parameters**

- base USART peripheral base address.
- data The byte to write.

static inline uint8\_t USART\_ReadByte(USART\_Type \*base)

Reads the RXDAT directly.

This function reads data from the RXDAT automatly. The upper layer must ensure that the RXDAT is not empty before calling this function.

#### **Parameters**

• base – USART peripheral base address.

# **Returns**

The byte read from USART data register.

status\_t USART WriteBlocking(USART\_Type \*base, const uint8\_t \*data, size\_t length)

Writes to the TX register using a blocking method.

This function polls the TX register, waits for the TX register to be empty.

## **Parameters**

- base USART peripheral base address.
- data Start address of the data to write.
- length Size of the data to write.

# **Return values**

- kStatus USART Timeout Transmission timed out and was aborted.
- kStatus Success Successfully wrote all data.

status\_t USART\_ReadBlocking(USART\_Type \*base, uint8\_t \*data, size\_t length)

Read RX data register using a blocking method.

This function polls the RX register, waits for the RX register to be full.

#### **Parameters**

- base USART peripheral base address.
- data Start address of the buffer to store the received data.

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• length – Size of the buffer.

#### **Return values**

- kStatus\_USART\_FramingError Receiver overrun happened while receiving data.
- kStatus\_USART\_ParityError Noise error happened while receiving data.
- kStatus\_USART\_NoiseError Framing error happened while receiving data.
- kStatus\_USART\_RxError Overflow or underflow happened.
- kStatus USART Timeout Transmission timed out and was aborted.
- kStatus Success Successfully received all data.

 $status\_t$  USART\_TransferCreateHandle(USART\_Type \*base,  $usart\_handle\_t$  \*handle,  $usart\_transfer\_callback\_t$  callback, void \*userData)

Initializes the USART handle.

This function initializes the USART handle which can be used for other USART transactional APIs. Usually, for a specified USART instance, call this API once to get the initialized handle.

#### **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.
- callback The callback function.
- userData The parameter of the callback function.

status\_t USART\_TransferSendNonBlocking(USART\_Type \*base, usart\_handle\_t \*handle, usart\_transfer t \*xfer)

Transmits a buffer of data using the interrupt method.

This function sends data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data to be written to the TX register. When all data is written to the TX register in the IRQ handler, the USART driver calls the callback function and passes the kStatus USART TxIdle as status parameter.

**Note:** The kStatus\_USART\_TxIdle is passed to the upper layer when all data is written to the TX register. However it does not ensure that all data are sent out. Before disabling the TX, check the kUSART TransmissionCompleteFlag to ensure that the TX is finished.

#### **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.
- xfer USART transfer structure. See usart\_transfer\_t.

# **Return values**

- kStatus Success Successfully start the data transmission.
- kStatus\_USART\_TxBusy Previous transmission still not finished, data not all written to TX register yet.
- kStatus InvalidArgument Invalid argument.

void USART\_TransferStartRingBuffer(USART\_Type \*base, usart\_handle\_t \*handle, uint8\_t \*ringBuffer, size\_t ringBufferSize)

Sets up the RX ring buffer.

This function sets up the RX ring buffer to a specific USART handle.

When the RX ring buffer is used, data received are stored into the ring buffer even when the user doesn't call the USART\_TransferReceiveNonBlocking() API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly.

**Note:** When using the RX ring buffer, one byte is reserved for internal use. In other words, if ringBufferSize is 32, then only 31 bytes are used for saving data.

#### **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.
- $\bullet \ {\rm ringBuffer}$  Start address of the ring buffer for background receiving. Pass NULL to disable the ring buffer.
- ringBufferSize size of the ring buffer.

void USART\_TransferStopRingBuffer(USART\_Type \*base, usart\_handle\_t \*handle)

Aborts the background transfer and uninstalls the ring buffer.

This function aborts the background transfer and uninstalls the ring buffer.

#### **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.

size\_t USART\_TransferGetRxRingBufferLength(usart\_handle\_t \*handle)

Get the length of received data in RX ring buffer.

# **Parameters**

• handle – USART handle pointer.

# Returns

Length of received data in RX ring buffer.

void USART\_TransferAbortSend(USART\_Type \*base, usart\_handle\_t \*handle)

Aborts the interrupt-driven data transmit.

This function aborts the interrupt driven data sending. The user can get the remainBtyes to find out how many bytes are still not sent out.

#### **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.

Get the number of bytes that have been written to USART TX register.

This function gets the number of bytes that have been written to USART TX register by interrupt method.

#### **Parameters**

• base – USART peripheral base address.

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- handle USART handle pointer.
- count Send bytes count.

## **Return values**

- kStatus\_NoTransferInProgress No send in progress.
- kStatus InvalidArgument Parameter is invalid.
- kStatus Success Get successfully through the parameter count;

 $status\_t$  USART\_TransferReceiveNonBlocking(USART\_Type \*base,  $usart\_handle\_t$  \*handle,  $usart\_transfer\_t$  \*xfer, size\_t \*receivedBytes)

Receives a buffer of data using an interrupt method.

This function receives data using an interrupt method. This is a non-blocking function, which returns without waiting for all data to be received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter <code>receivedBytes</code> shows how many bytes are copied from the ring buffer. After copying, if the data in the ring buffer is not enough to read, the receive request is saved by the USART driver. When the new data arrives, the receive request is serviced first. When all data is received, the USART driver notifies the upper layer through a callback function and passes the status parameter kStatus\_USART\_RxIdle. For example, the upper layer needs 10 bytes but there are only 5 bytes in the ring buffer. The 5 bytes are copied to the xfer->data and this function returns with the parameter <code>receivedBytes</code> set to 5. For the left 5 bytes, newly arrived data is saved from the xfer->data[5]. When 5 bytes are received, the USART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to the xfer->data. When all data is received, the upper layer is notified.

#### **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.
- xfer USART transfer structure, see usart\_transfer\_t.
- receivedBytes Bytes received from the ring buffer directly.

# **Return values**

- kStatus Success Successfully queue the transfer into transmit queue.
- kStatus\_USART\_RxBusy Previous receive request is not finished.
- kStatus\_InvalidArgument Invalid argument.

void USART\_TransferAbortReceive(USART\_Type \*base, usart\_handle\_t \*handle)

Aborts the interrupt-driven data receiving.

This function aborts the interrupt-driven data receiving. The user can get the remainBytes to find out how many bytes not received yet.

# **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.

Get the number of bytes that have been received.

This function gets the number of bytes that have been received.

#### **Parameters**

• base – USART peripheral base address.

- handle USART handle pointer.
- count Receive bytes count.

#### **Return values**

- kStatus\_NoTransferInProgress No receive in progress.
- kStatus InvalidArgument Parameter is invalid.
- kStatus\_Success Get successfully through the parameter count;

void USART\_TransferHandleIRQ(USART\_Type \*base, usart\_handle\_t \*handle) USART IRQ handle function.

This function handles the USART transmit and receive IRQ request.

## **Parameters**

- base USART peripheral base address.
- handle USART handle pointer.

FSL\_USART\_DRIVER\_VERSION USART driver version.

Error codes for the USART driver.

Values:

enumerator kStatus\_USART\_TxBusy Transmitter is busy.

enumerator kStatus\_USART\_RxBusy Receiver is busy.

 ${\bf enumerator} \ {\rm kStatus\_USART\_TxIdle}$ 

USART transmitter is idle.

enumerator kStatus\_USART\_RxIdle USART receiver is idle.

enumerator kStatus\_USART\_TxError

Error happens on tx.
enumerator kStatus\_USART\_RxError

Error happens on rx.

 ${\bf enumerator} \ {\bf kStatus\_USART\_RxRingBufferOverrun}$ 

Error happens on rx ring buffer

enumerator kStatus\_USART\_NoiseError

USART noise error.

enumerator kStatus\_USART\_FramingError USART framing error.

enumerator kStatus\_USART\_ParityError USART parity error.

enumerator kStatus\_USART\_HardwareOverrun

enumerator kStatus\_USART\_BaudrateNotSupport

USART hardware over flow.

Baudrate is not support in current clock source

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```
enumerator kStatus_USART_Timeout
         USART times out.
enum _usart_parity_mode
    USART parity mode.
    Values:
    enumerator kUSART ParityDisabled
         Parity disabled
    enumerator kUSART_ParityEven
         Parity enabled, type even, bit setting: PARITYSEL = 10
    enumerator kUSART ParityOdd
         Parity enabled, type odd, bit setting: PARITYSEL = 11
enum usart sync mode
    USART synchronous mode.
    Values:
    enumerator kUSART SyncModeDisabled
         Asynchronous mode.
    enumerator kUSART_SyncModeSlave
         Synchronous slave mode.
    enumerator kUSART_SyncModeMaster
         Synchronous master mode.
enum _usart_stop_bit_count
    USART stop bit count.
    Values:
    enumerator kUSART_OneStopBit
         One stop bit
    enumerator kUSART_TwoStopBit
         Two stop bits
enum usart data len
    USART data size.
     Values:
    enumerator kUSART 7BitsPerChar
         Seven bit mode
    enumerator kUSART_8BitsPerChar
         Eight bit mode
enum _usart_clock_polarity
    USART clock polarity configuration, used in sync mode.
    Values:
    enumerator~{\rm kUSART\_RxSampleOnFallingEdge}
         Un_RXD is sampled on the falling edge of SCLK.
    enumerator kUSART_RxSampleOnRisingEdge
         Un_RXD is sampled on the rising edge of SCLK.
```

```
enum \_usart\_interrupt\_enable
     USART interrupt configuration structure, default settings all disabled.
     Values:
     enumerator kUSART RxReadyInterruptEnable
         Receive ready interrupt.
     enumerator kUSART TxReadyInterruptEnable
         Transmit ready interrupt.
     enumerator kUSART_TxIdleInterruptEnable
         Transmit idle interrupt.
     enumerator kUSART DeltaCtsInterruptEnable
         Cts pin change interrupt.
     enumerator kUSART TxDisableInterruptEnable
         Transmit disable interrupt.
     enumerator kUSART HardwareOverRunInterruptEnable
         hardware ove run interrupt.
     {\bf enumerator} \ {\bf kUSART\_RxBreakInterruptEnable}
         Receive break interrupt.
     enumerator kUSART RxStartInterruptEnable
         Receive ready interrupt.
     enumerator kUSART FramErrorInterruptEnable
         Receive start interrupt.
     enumerator kUSART ParityErrorInterruptEnable
         Receive frame error interrupt.
     enumerator kUSART RxNoiseInterruptEnable
         Receive noise error interrupt.
     enumerator kUSART AutoBaudErrorInterruptEnable
         Receive auto baud error interrupt.
     enumerator kUSART AllInterruptEnable
         All interrupt.
enum _usart_flags
     USART status flags.
     This provides constants for the USART status flags for use in the USART functions.
     Values:
     enumerator kUSART RxReady
         Receive ready flag.
     enumerator kUSART_RxIdleFlag
         Receive IDLE flag.
     enumerator kUSART_TxReady
         Transmit ready flag.
     enumerator kUSART_TxIdleFlag
         Transmit idle flag.
```

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```
enumerator~{\rm kUSART\_CtsState}
         Cts pin status.
     enumerator kUSART_DeltaCtsFlag
         Cts pin change flag.
     enumerator kUSART_TxDisableFlag
         Transmit disable flag.
     enumerator kUSART_HardwareOverrunFlag
         Hardware over run flag.
     enumerator kUSART RxBreakFlag
         Receive break flag.
     enumerator kUSART RxStartFlag
         receive start flag.
     enumerator kUSART_FramErrorFlag
         Frame error flag.
     enumerator kUSART ParityErrorFlag
         Parity error flag.
     enumerator kUSART_RxNoiseFlag
         Receive noise flag.
     enumerator kUSART_AutoBaudErrorFlag
         Auto baud error flag.
typedef enum _usart_parity_mode usart_parity_mode_t
    USART parity mode.
typedef enum _usart_sync_mode usart_sync_mode_t
    USART synchronous mode.
typedef enum _usart_stop_bit_count usart_stop_bit_count_t
    USART stop bit count.
typedef enum _usart_data_len usart_data_len_t
    USART data size.
typedef enum _usart_clock_polarity usart_clock_polarity_t
    USART clock polarity configuration, used in sync mode.
typedef struct _usart_config usart_config_t
    USART configuration structure.
typedef struct _usart_transfer usart_transfer_t
    USART transfer structure.
typedef struct_usart_handle usart_handle_t
typedef void (*usart_transfer_callback_t)(USART_Type *base, usart_handle_t *handle, status_t
status, void *userData)
    USART transfer callback function.
FSL SDK ENABLE USART DRIVER TRANSACTIONAL APIS
    Macro gate for enable transaction API. 1 for enable, 0 for disable.
FSL SDK USART DRIVER ENABLE BAUDRATE AUTO GENERATE
    USART baud rate auto generate switch gate. 1 for enable, 0 for disable.
```

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# UART\_RETRY\_TIMES

Retry times for waiting flag.

Defining to zero means to keep waiting for the flag until it is assert/deassert.

struct usart config

#include <fsl\_usart.h> USART configuration structure.

#### **Public Members**

uint32\_t baudRate Bps

**USART** baud rate

bool enableRx

USART receive enable.

bool enableTx

USART transmit enable.

bool loopback

Enable peripheral loopback

bool enableContinuousSCLK

USART continuous Clock generation enable in synchronous master mode.

bool enableHardwareFlowControl

Enable hardware control RTS/CTS

usart\_parity\_mode\_t parityMode

Parity mode, disabled (default), even, odd

usart\_stop\_bit\_count\_t stopBitCount

Number of stop bits, 1 stop bit (default) or 2 stop bits

usart\_data\_len\_t bitCountPerChar

Data length - 7 bit, 8 bit

usart\_sync\_mode\_t syncMode

Transfer mode - asynchronous, synchronous master, synchronous slave.

usart\_clock\_polarity\_t clockPolarity

Selects the clock polarity and sampling edge in sync mode.

struct \_usart\_transfer

#include <fsl\_usart.h> USART transfer structure.

# **Public Members**

size t dataSize

The byte count to be transfer.

struct usart handle

#include <fsl\_usart.h> USART handle structure.

#### **Public Members**

const uint8\_t \*volatile txData

Address of remaining data to send.

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```
volatile size_t txDataSize
          Size of the remaining data to send.
     size_t txDataSizeAll
          Size of the data to send out.
     uint8 t *volatile rxData
          Address of remaining data to receive.
     volatile size_t rxDataSize
          Size of the remaining data to receive.
     size_t rxDataSizeAll
          Size of the data to receive.
     uint8 t *rxRingBuffer
          Start address of the receiver ring buffer.
     size_t rxRingBufferSize
          Size of the ring buffer.
     volatile uint16_t rxRingBufferHead
          Index for the driver to store received data into ring buffer.
     volatile uint16_t rxRingBufferTail
          Index for the user to get data from the ring buffer.
     usart transfer callback t callback
          Callback function.
     void *userData
          USART callback function parameter.
     volatile uint8 t txState
          TX transfer state.
     volatile uint8 t rxState
          RX transfer state
union unnamed6
     Public Members
     uint8 t*data
          The buffer of data to be transfer.
     uint8_t *rxData
          The buffer to receive data.
     const uint8 t*txData
          The buffer of data to be sent.
```

# 2.24 WKT: Self-wake-up Timer

void WKT\_Init(WKT\_Type \*base, const wkt\_config\_t \*config)

Ungates the WKT clock and configures the peripheral for basic operation.

**Note:** This API should be called at the beginning of the application using the WKT driver.

#### **Parameters**

- base WKT peripheral base address
- config Pointer to user's WKT config structure.

void WKT Deinit(WKT Type \*base)

Gate the WKT clock.

#### **Parameters**

• base – WKT peripheral base address

static inline void WKT\_GetDefaultConfig(wkt\_config\_t \*config)

Initializes the WKT configuration structure.

This function initializes the WKT configuration structure to default values. The default values are as follows.

 $config->clockSource = kWKT\_DividedFROClockSource;$ 

#### See also:

wkt\_config\_t

#### **Parameters**

• config – Pointer to the WKT configuration structure.

static inline uint32\_t WKT\_GetCounterValue(WKT\_Type \*base)

Read actual WKT counter value.

#### **Parameters**

• base – WKT peripheral base address

static inline uint32\_t WKT GetStatusFlags(WKT\_Type \*base)

Gets the WKT status flags.

# **Parameters**

• base – WKT peripheral base address

# Returns

The status flags. This is the logical OR of members of the enumeration wkt status flags t

static inline void WKT\_ClearStatusFlags(WKT\_Type \*base, uint32\_t mask)

Clears the WKT status flags.

# **Parameters**

- base WKT peripheral base address
- mask The status flags to clear. This is a logical OR of members of the enumeration wkt\_status\_flags\_t

static inline void WKT StartTimer(WKT\_Type \*base, uint32\_t count)

Starts the timer counting.

After calling this function, timer loads a count value, counts down to 0, then stops.

**Note:** User can call the utility macros provided in fsl\_common.h to convert to ticks Do not write to Counter register while the counting is in progress

#### **Parameters**

- base WKT peripheral base address.
- count The value to be loaded into the WKT Count register

static inline void WKT\_StopTimer(WKT\_Type \*base)

Stops the timer counting.

This function Clears the counter and stops the timer from counting.

# **Parameters**

• base – WKT peripheral base address

FSL\_WKT\_DRIVER\_VERSION

Version 2.0.2

enum wkt clock source

Describes WKT clock source.

Values:

enumerator kWKT DividedFROClockSource

WKT clock sourced from the divided FRO clock

enumerator kWKT LowPowerClockSource

WKT clock sourced from the Low power clock Use this clock, LPOSCEN bit of DPDCTRL register must be enabled

enumerator kWKT ExternalClockSource

WKT clock sourced from the Low power clock Use this clock, WAKECLKPAD\_DISABLE bit of DPDCTRL register must be enabled

enum \_wkt\_status\_flags

List of WKT flags.

Values:

enumerator kWKT\_AlarmFlag

Alarm flag

typedef enum \_wkt\_clock\_source wkt\_clock\_source\_t

Describes WKT clock source.

typedef struct\_wkt\_config\_wkt\_config\_t

Describes WKT configuration structure.

typedef enum \_wkt\_status\_flags wkt\_status\_flags\_t

List of WKT flags.

struct \_wkt\_config

#include <fsl\_wkt.h> Describes WKT configuration structure.

# **Public Members**

wkt\_clock\_source\_t clockSource

External or internal clock source select

# 2.25 WWDT: Windowed Watchdog Timer Driver

void WWDT\_GetDefaultConfig(wwdt\_config\_t \*config)

Initializes WWDT configure structure.

This function initializes the WWDT configure structure to default value. The default value are:

```
config->enableWwdt = true;

config->enableWatchdogReset = false;

config->enableWatchdogProtect = false;

config->enableLockOscillator = false;

config->windowValue = 0xFFFFFFU;

config->timeoutValue = 0xFFFFFFU;

config->warningValue = 0;
```

#### See also:

wwdt\_config\_t

# **Parameters**

config – Pointer to WWDT config structure.

void WWDT\_Init(WWDT\_Type \*base, const wwdt\_config\_t \*config)

Initializes the WWDT.

This function initializes the WWDT. When called, the WWDT runs according to the configuration.

Example:

```
wwdt_config_t config;
WWDT_GetDefaultConfig(&config);
config.timeoutValue = 0x7ffU;
WWDT_Init(wwdt_base,&config);
```

# **Parameters**

- base WWDT peripheral base address
- config The configuration of WWDT

void WWDT Deinit(WWDT\_Type \*base)

Shuts down the WWDT.

This function shuts down the WWDT.

#### **Parameters**

• base – WWDT peripheral base address

static inline void WWDT\_Enable(WWDT\_Type \*base)

Enables the WWDT module.

This function write value into WWDT\_MOD register to enable the WWDT, it is a write-once bit; once this bit is set to one and a watchdog feed is performed, the watchdog timer will run permanently.

## **Parameters**

• base – WWDT peripheral base address

static inline void WWDT Disable(WWDT\_Type \*base)

Disables the WWDT module.

## Deprecated:

Do not use this function. It will be deleted in next release version, for once the bit field of WDEN written with a 1, it can not be re-written with a 0.

This function write value into WWDT\_MOD register to disable the WWDT.

#### **Parameters**

• base – WWDT peripheral base address

 $static\ in line\ uint 32\_t\ \mathrm{WWDT\_GetStatusFlags}(WWDT\_Type\ *base)$ 

Gets all WWDT status flags.

This function gets all status flags.

Example for getting Timeout Flag:

```
uint32_t status;
status = WWDT_GetStatusFlags(wwdt_base) & kWWDT_TimeoutFlag;
```

#### **Parameters**

• base – WWDT peripheral base address

#### Returns

The status flags. This is the logical OR of members of the enumeration \_wwdt\_status\_flags\_t

void WWDT\_ClearStatusFlags(WWDT\_Type \*base, uint32\_t mask)

Clear WWDT flag.

This function clears WWDT status flag.

Example for clearing warning flag:

```
WWDT ClearStatusFlags(wwdt base, kWWDT WarningFlag);
```

## **Parameters**

- base WWDT peripheral base address
- mask The status flags to clear. This is a logical OR of members of the enumeration \_wwdt\_status\_flags\_t

static inline void WWDT\_SetWarningValue(WWDT\_Type \*base, uint32\_t warningValue) Set the WWDT warning value.

The WDWARNINT register determines the watchdog timer counter value that will generate a watchdog interrupt. When the watchdog timer counter is no longer greater than the value defined by WARNINT, an interrupt will be generated after the subsequent WDCLK.

#### **Parameters**

- base WWDT peripheral base address
- warningValue WWDT warning value.

static inline void WWDT\_SetTimeoutValue(WWDT\_Type \*base, uint32\_t timeoutCount)

Set the WWDT timeout value.

This function sets the timeout value. Every time a feed sequence occurs the value in the TC register is loaded into the Watchdog timer. Writing a value below 0xFF will cause 0xFF to be

loaded into the TC register. Thus the minimum time-out interval is TWDCLK\*256\*4. If enableWatchdogProtect flag is true in wwdt\_config\_t config structure, any attempt to change the timeout value before the watchdog counter is below the warning and window values will cause a watchdog reset and set the WDTOF flag.

#### **Parameters**

- base WWDT peripheral base address
- timeoutCount WWDT timeout value, count of WWDT clock tick.

static inline void WWDT\_SetWindowValue(WWDT\_Type \*base, uint32\_t windowValue)

Sets the WWDT window value.

The WINDOW register determines the highest TV value allowed when a watchdog feed is performed. If a feed sequence occurs when timer value is greater than the value in WINDOW, a watchdog event will occur. To disable windowing, set windowValue to 0xFFFFFF (maximum possible timer value) so windowing is not in effect.

#### **Parameters**

- base WWDT peripheral base address
- windowValue WWDT window value.

void WWDT\_Refresh(WWDT\_Type \*base)

Refreshes the WWDT timer.

This function feeds the WWDT. This function should be called before WWDT timer is in timeout. Otherwise, a reset is asserted.

#### **Parameters**

• base – WWDT peripheral base address

FSL WWDT DRIVER VERSION

Defines WWDT driver version.

WWDT FIRST WORD OF REFRESH

First word of refresh sequence

WWDT SECOND WORD OF REFRESH

Second word of refresh sequence

 $enum \_wwdt\_status\_flags\_t$ 

WWDT status flags.

This structure contains the WWDT status flags for use in the WWDT functions.

Values:

enumerator kWWDT TimeoutFlag

Time-out flag, set when the timer times out

enumerator kWWDT WarningFlag

Warning interrupt flag, set when timer is below the value WDWARNINT

typedef struct \_wwdt\_config wwdt\_config\_t

Describes WWDT configuration structure.

struct wwdt config

#include <fsl\_wwdt.h> Describes WWDT configuration structure.

## **Public Members**

bool enableWwdt

**Enables or disables WWDT** 

bool enableWatchdogReset

true: Watchdog timeout will cause a chip reset false: Watchdog timeout will not cause a chip reset

 $\boldsymbol{bool}\ \mathbf{enableWatchdogProtect}$ 

true: Enable watchdog protect i.e timeout value can only be changed after counter is below warning & window values false: Disable watchdog protect; timeout value can be changed at any time

bool enableLockOscillator

true: Disabling or powering down the watchdog oscillator is prevented Once set, this bit can only be cleared by a reset false: Do not lock oscillator

uint32 t windowValue

Window value, set this to 0xFFFFFF if windowing is not in effect

 $uint32\_t \ \mathrm{timeoutValue}$ 

Timeout value

uint32\_t warningValue

Watchdog time counter value that will generate a warning interrupt. Set this to 0 for no warning

 $uint32\_t \; {\rm clockFreq\_Hz}$ 

Watchdog clock source frequency.

# **Chapter 3**

# **Middleware**

# 3.1 Motor Control

# 3.1.1 FreeMASTER

Communication Driver User Guide

### Introduction

**What is FreeMASTER?** FreeMASTER is a PC-based application developed by NXP for NXP customers. It is a versatile tool usable as a real-time monitor, visualization tool, and a graphical control panel of embedded applications based on the NXP processing units.

This document describes the embedded-side software driver which implements an interface between the application and the host PC. The interface covers the following communication:

- **Serial** UART communication either over plain RS232 interface or more typically over a USB-to-Serial either external or built in a debugger probe.
- USB direct connection to target microcontroller
- · CAN bus
- TCP/IP network wired or WiFi
- Segger J-Link RTT
- JTAG debug port communication
- ...and all of the above also using a **Zephyr** generic drivers.

The driver also supports so-called "packet-driven BDM" interface which enables a protocol-based communication over a debugging port. The BDM stands for Background Debugging Module and its physical implementation is different on each platform. Some platforms leverage a semistandard JTAG interface, other platforms provide a custom implementation called BDM. Regardless of the name, this debugging interface enables non-intrusive access to the memory space while the target CPU is running. For basic memory read and write operations, there is no communication driver required on the target when communicating with the host PC. Use this driver to get more advanced FreeMASTER protocol features over the BDM interface. The driver must be configured for the packet-driven BDM mode, in which the host PC uses the debugging interface to write serial command frames directly to the target memory buffer. The same method is then used to read response frames from that memory buffer.

Similar to "packet-driven BDM", the FreeMASTER also supports a communication over [J-Link RTT]((https://www.segger.com/products/debug-probes/j-link/technology/about-real-time-transfer/) interface defined by SEGGER Microcontroller GmbH for ARM CortexM-based microcontrollers. This method also uses JTAG physical interface and enables high-speed real time communication to run over the same channel as used for application debugging.

**Driver version 3** This document describes version 3 of the FreeMASTER Communication Driver. This version features the implementation of the new Serial Protocol, which significantly extends the features and security of its predecessor. The new protocol internal number is v4 and its specification is available in the documentation accompanying the driver code.

Driver V3 is deployed to modern 32-bit MCU platforms first, so the portfolio of supported platforms is smaller than for the previous V2 versions. It is recommended to keep using the V2 driver for legacy platforms, such as S08, S12, ColdFire, or Power Architecture. Reach out to FreeMAS-TER community or to the local NXP representative with requests for more information or to port the V3 driver to legacy MCU devices.

Thanks to a layered approach, the new driver simplifies the porting of the driver to new UART, CAN or networking communication interfaces significantly. Users are encouraged to port the driver to more NXP MCU platforms and contribute the code back to NXP for integration into future releases. Existing code and low-level driver layers may be used as an example when porting to new targets.

**Note:** Using the FreeMASTER tool and FreeMASTER Communication Driver is only allowed in systems based on NXP microcontroller or microprocessor unit. Use with non-NXP MCU platforms is **not permitted** by the license terms.

**Target platforms** The driver implementation uses the following abstraction mechanisms which simplify driver porting and supporting new communication modules:

- **General CPU Platform** (see source code in the src/platforms directory). The code in this layer is only specific to native data type sizes and CPU architectures (for example; alignment-aware memory copy routines). This driver version brings two generic implementations of 32-bit platforms supporting both little-endian and big-endian architectures. There are also implementations customized for the 56F800E family of digital signal controllers and S12Z MCUs. **Zephyr** is treated as a specific CPU platform as it brings unified user configuration (Kconfig) and generic hardware device drivers. With Zephyr, the transport layer and low-level communication layers described below are configured automatically using Kconfig and Device Tree technologies.
- Transport Communication Layer The Serial, CAN, Networking, PD-BDM, and other methods of transport logic are implemented as a driver layer called FMSTR\_TRANSPORT with a uniform API. A support of the Network transport also extends single-client modes of operation which are native for Serial, USB and CAN by a concept of multiple client sessions.
- Low-level Communication Driver Each type of transport further defines a low-level API used to access the physical communication module. For example, the Serial transport defines a character-oriented API implemented by different serial communication modules like UART, LPUART, USART, and also USB-CDC. Similarly, the CAN transport defines a message-oriented API implemented by the FlexCAN or MCAN modules. Moreover, there are multiple different implementations for the same kind of communication peripherals. The difference between the implementation is in the way the low-level hardware registers are accessed. The mcuxsdk folder contains implementations which use MCUXpresso SDK drivers. These drivers should be used in applications based on the NXP MCUXpresso SDK. The "ampsdk" drivers target automotive-specific MCUs and their respective SDKs. The "dreg" implementations use a plain C-language access to hardware register addresses which makes it a universal and the most portable solution. In this case, users are encouraged to add more drivers for other communication modules or other respective SDKs and contribute the code back to NXP for integration.

The low-level drivers defined for the Networking transport enable datagram-oriented UDP and stream TCP communication. This implementation is demonstrated using the lwIP software stack but shall be portable to other TCP/IP stacks. It may sound surprisingly, but also the Segger J-Link RTT communication driver is linked to the Networking transport (RTT is stream oriented communication handled similarly to TCP).

**Replacing existing drivers** For all supported platforms, the driver described in this document replaces the V2 implementation and also older driver implementations that were available separately for individual platforms (PC Master SCI drivers).

**Clocks**, **pins**, **and peripheral initialization** The FreeMASTER communication driver is only responsible for runtime processing of the communication and must be integrated with an user application code to function properly. The user application code is responsible for general initialization of clock sources, pin multiplexers, and peripheral registers related to the communication speed. Such initialization should be done before calling the FMSTR\_Init function.

It is recommended to develop the user application using one of the Software Development Kits (SDKs) available from third parties or directly from NXP, such as MCUXpresso SDK, MCUXpresso IDE, and related tools. This approach simplifies the general configuration process significantly.

**MCUXpresso SDK** The MCUXpresso SDK is a software package provided by NXP which contains the device initialization code, linker files, and software drivers with example applications for the NXP family of MCUs. The MCUXpresso Config Tools may be used to generate the clock-setup and pin-multiplexer setup code suitable for the selected processor.

The MCUXpresso SDK also contains this FreeMASTER communication driver as a "middle-ware" component which may be downloaded along with the example applications from https://mcuxpresso.nxp.com/en/welcome.

**MCUXpresso SDK on GitHub** The FreeMASTER communication driver is also released as one of the middleware components of the MCUXpresso SDK on the GitHub. This release enables direct integration of the FreeMASTER source code Git repository into a target applications including Zephyr applications.

# Related links:

- The official FreeMASTER middleware repository.
- Online version of this document

**FreeMASTER in Zephyr** The FreeMASTER middleware repository can be used with MCUX-presso SDK as well as a Zephyr module. Zephyr-specific samples which include examples of Kconfig and Device Tree configurations for Serial, USB and Network communications are available in separate repository. West manifest in this sample repository fetches the full Zephyr package including the FreeMASTER middleware repository used as a Zephyr module.

# **Example applications**

**MCUX SDK Example applications** There are several example applications available for each supported MCU platform.

• **fmstr\_uart** demonstrates a plain serial transmission, typically connecting to a computer's physical or virtual COM port. The typical transmission speed is 115200 bps.

- fmstr\_can demonstrates CAN bus communication. This requires a suitable CAN interface connected to the computer and interconnected with the target MCU using a properly terminated CAN bus. The typical transmission speed is 500 kbps. A FreeMASTER-over-CAN communication plug-in must be used.
- fmstr\_usb\_cdc uses an on-chip USB controller to implement a CDC communication class. It is connected directly to a computer's USB port and creates a virtual COM port device. The typical transmission speed is above 1 Mbps.
- fmstr\_net demonstrates the Network communication over UDP or TCP protocol. Existing examples use lwIP stack to implement the communication, but in general, it shall be possible to use any other TCP/IP stack to achieve the same functionality.
- **fmstr\_wifi** is the fmstr\_net application modified to use a WiFi network interface instead of a wired Ethernet connection.
- fmstr\_rtt demonstrates the communication over SEGGER J-Link RTT interface. Both fmstr\_net and fmstr\_rtt examples require the FreeMASTER TCP/UDP communication plug-in to be used on the PC host side.
- fmstr\_eonce uses the real-time data unit on the JTAG EOnCE module of the 56F800E family to implement pseudo-serial communication over the JTAG port. The typical transmission speed is around 10 kbps. This communication requires FreeMASTER JTAG/EOnCE communication plug-in.
- fmstr\_pdbdm uses JTAG or BDM debugging interface to access the target RAM directly while the CPU is running. Note that such approach can be used with any MCU application, even without any special driver code. The computer reads from and writes into the RAM directly without CPU intervention. The Packet-Driven BDM (PD-BDM) communication uses the same memory access to exchange command and response frames. With PD-BDM, the FreeMASTER tool is able to go beyond basic memory read/write operations and accesses also advanced features like Recorder, TSA, or Pipes. The typical transmission speed is around 10 kbps. A PD-BDM communication plug-in must be used in FreeMASTER and configured properly for the selected debugging interface. Note that this communication cannot be used while a debugging interface is used by a debugger session.
- **fmstr\_any** is a special example application which demonstrates how the NXP MCUXpresso Config Tools can be used to configure pins, clocks, peripherals, interrupts, and even the FreeMASTER "middleware" driver features in a graphical and user friendly way. The user can switch between the Serial, CAN, and other ways of communication and generate the required initialization code automatically.

**Zephyr sample spplications** Zephyr sample applications demonstrate Kconfig and Device Tree configuration which configure the FreeMASTER middleware module for a selected communication option (Serial, CAN, Network or RTT).

Refer to *readme.md* files in each sample directory for description of configuration options required to implement FreeMASTER connectivity.

# **Description**

This section shows how to add the FreeMASTER Communication Driver into application and how to configure the connection to the FreeMASTER visualization tool.

**Features** The FreeMASTER driver implements the FreeMASTER protocol V4 and provides the following features which may be accessed using the FreeMASTER visualization tool:

- Read/write access to any memory location on the target.
- Optional password protection of the read, read/write, and read/write/flash access levels.

- Atomic bit manipulation on the target memory (bit-wise write access).
- Optimal size-aligned access to memory which is also suitable to access the peripheral register space.
- Oscilloscope access—real-time access to target variables. The sample rate may be limited by the communication speed.
- Recorder— access to the fast transient recorder running on the board as a part of the FreeMASTER driver. The sample rate is only limited by the MCU CPU speed. The length of the data recorded depends on the amount of available memory.
- Multiple instances of Oscilloscopes and Recorders without the limitation of maximum number of variables.
- Application commands—high-level message delivery from the PC to the application.
- TSA tables—describing the data types, variables, files, or hyperlinks exported by the target application. The TSA newly supports also non-memory mapped resources like external EEPROM or SD Card files.
- Pipes—enabling the buffered stream-oriented data exchange for a general-purpose terminal-like communication, diagnostic data streaming, or other data exchange.

#### The FreeMASTER driver features:

- Full FreeMASTER protocol V4 implementation with a new V4 style of CRC used.
- Layered approach supporting Serial, CAN, Network, PD-BDM, and other transports.
- Layered low-level Serial transport driver architecture enabling to select UART, LPUART, USART, and other physical implementations of serial interfaces, including USB-CDC.
- Layered low-level CAN transport driver architecture enabling to select FlexCAN, msCAN, MCAN, and other physical implementations of the CAN interface.
- Layered low-level Networking transport enabling to select TCP, UDP or J-Link RTT communication.
- TSA support to write-protect memory regions or individual variables and to deny the access to the unsafe memory.
- The pipe callback handlers are invoked whenever new data is available for reading from the pipe.
- Two Serial Single-Wire modes of operation are enabled. The "external" mode has the RX and TX shorted on-board. The "true" single-wire mode interconnects internally when the MCU or UART modules support it.

The following sections briefly describe all FreeMASTER features implemented by the driver. See the PC-based FreeMASTER User Manual for more details on how to use the features to monitor, tune, or control an embedded application.

**Board Detection** The FreeMASTER protocol V4 defines the standard set of configuration values which the host PC tool reads to identify the target and to access other target resources properly. The configuration includes the following parameters:

- Version of the driver and the version of the protocol implemented.
- MTU as the Maximum size of the Transmission Unit (for example; communication buffer size).
- Application name, description, and version strings.
- · Application build date and time as a string.
- Target processor byte ordering (little/big endian).
- Protection level that requires password authentication.

- Number of the Recorder and Oscilloscope instances.
- RAM Base Address for optimized memory access commands.

**Memory Read** This basic feature enables the host PC to read any data memory location by specifying the address and size of the required memory area. The device response frame must be shorter than the MTU to fit into the outgoing communication buffer. To read a device memory of any size, the host uses the information retrieved during the Board Detection and splits the large-block request to multiple partial requests.

The driver uses size-aligned operations to read the target memory (for example; uses proper read-word instruction when an address is aligned to 4 bytes).

**Memory Write** Similarly to the Memory Read operation, the Memory Write feature enables to write to any RAM memory location on the target device. A single write command frame must be shorter than the MTU to fit into the target communication buffer. Larger requests must be split into smaller ones.

The driver uses size-aligned operations to write to the target memory (for example; uses proper write-word instruction when an address is aligned to 4 bytes).

**Masked Memory Write** To implement the write access to a single bit or a group of bits of target variables, the Masked Memory Write feature is available in the FreeMASTER protocol and it is supported by the driver using the Read-Modify-Write approach.

Be careful when writing to bit fields of volatile variables that are also modified in an application interrupt. The interrupt may be serviced in the middle of a read-modify-write operation and it may cause data corruption.

**Oscilloscope** The protocol and driver enables any number of variables to be read at once with a single request from the host. This feature is called Oscilloscope and the FreeMASTER tool uses it to display a real-time graph of variable values.

The driver can be configured to support any number of Oscilloscope instances and enable simultaneously running graphs to be displayed on the host computer screen.

**Recorder** The protocol enables the host to select target variables whose values are then periodically recorded into a dedicated on-board memory buffer. After such data sampling stops (either on a host request or by evaluating a threshold-crossing condition), the data buffer is downloaded to the host and displayed as a graph. The data sampling rate is not limited by the speed of the communication line, so it enables displaying the variable transitions in a very high resolution.

The driver can be configured to support multiple Recorder instances and enable multiple recorder graphs to be displayed on the host screen. Having multiple recorders also enables setting the recording point differently for each instance. For example; one instance may be recording data in a general timer interrupt while another instance may record at a specific control algorithm time in the PWM interrupt.

**TSA** With the TSA feature, data types and variables can be described directly in the application source code. Such information is later provided to the FreeMASTER tool which may use it instead of reading symbol data from the application ELF executable file.

The information is encoded as so-called TSA tables which become direct part of the application code. The TSA tables contain descriptors of variables that shall be visible to the host tool. The descriptors can describe the memory areas by specifying the address and size of the memory

block or more conveniently using the C variable names directly. Different set of TSA descriptors can be used to encode information about the structure types, unions, enumerations, or arrays.

The driver also supports special types of TSA table entries to describe user resources like external EEPROM and SD Card files, memory-mapped files, virtual directories, web URL hyperlinks, and constant enumerations.

**TSA Safety** When the TSA is enabled in the application, the TSA Safety can be enabled and validate the memory accesses directly by the embedded-side driver. When the TSA Safety is turned on, any memory request received from the host is validated and accepted only if it belongs to a TSA-described object. The TSA entries can be declared as Read-Write or Read-Only so that the driver can actively deny the write access to the Read-Only objects.

**Application commands** The Application Commands are high-level messages that can be delivered from the PC Host to the embedded application for further processing. The embedded application can either poll the status, or be called back when a new Application Command arrives to be processed. After the embedded application acknowledges that the command is handled, the host receives the Result Code and reads the other return data from memory. Both the Application Commands and the Result Codes are specific to a given application and it is user's responsibility to define them. The FreeMASTER protocol and the FreeMASTER driver only implement the delivery channel and a set of API calls to enable the Application Command processing in general.

**Pipes** The Pipes enable buffered and stream-oriented data exchange between the PC Host and the target application. Any pipe can be written to and read from at both ends (either on the PC or the MCU). The data transmission is acknowledged using the special FreeMASTER protocol commands. It is guaranteed that the data bytes are delivered from the writer to the reader in a proper order and without losses.

**Serial single-wire operation** The MCU Serial Communication Driver natively supports normal dual-wire operation. Because the protocol is half-duplex only, the driver can also operate in two single-wire modes:

- "External" single-wire operation where the Receiver and Transmitter pins are shorted on the board. This mode is supported by default in the MCU driver because the Receiver and Transmitter units are enabled or disabled whenever needed. It is also easy to extend this operation for the RS485 communication.
- "True" single-wire mode which uses only a single pin and the direction switching is made by the UART module. This mode of operation must be enabled by defining the FM-STR\_SERIAL\_SINGLEWIRE configuration option.

**Multi-session support** With networking interface it is possible for multiple clients to access the target MCU simultaneously. Reading and writing of target memory is processed atomically so there is no risk of data corruption. The state-full resources such as Recorders or Oscilloscopes are locked to a client session upon first use and access is denied to other clients until lock is released..

**Zephyr-specific** 

**Dedicated communication task** FreeMASTER communication may run isolated in a dedicated task. The task automates the FMSTR\_Init and FMSTR\_Poll calls together with periodic activities enabling the FreeMASTER UI to fetch information about tasks and CPU utilization. The task can be started automatically or manually, and it must be assigned a priority to be able to react on interrupts and other communication events. Refer to Zephyr FreeMASTER sample applications which all use this communication task.

**Zephyr shell and logging over FreeMASTER pipe** FreeMASTER implements a shell backend which may use FreeMASTER pipe as a I/O terminal and logging output. Refer to Zephyr FreeMASTER sample applications which all use this feature.

**Automatic TSA tables** TSA tables can be declared as "automatic" in Zephyr which make them automatically registered in the table list. This may be very useful when there are many TSA tables or when the tables are defined in different (often unrelated) libraries linked together. In this case user does not need to build a list of all tables manually.

**Driver files** The driver source files can be found in a top-level src folder, further divided into the sub-folders:

- *src/platforms* platform-specific folder—one folder exists for each supported processor platform (for example; 32-bit Little Endian platform). Each such folder contains a platform header file with data types and a code which implements the potentially platform-specific operations, such as aligned memory access.
- *src/common* folder—contains the common driver source files shared by the driver for all supported platforms. All the .*c* files must be added to the project, compiled, and linked together with the application.
  - freemaster.h master driver header file, which declares the common data types, macros, and prototypes of the FreeMASTER driver API functions.
  - freemaster\_cfg.h.example this file can serve as an example of the FreeMASTER driver configuration file. Save this file into a project source code folder and rename it to freemaster\_cfg.h. The FreeMASTER driver code includes this file to get the project-specific configuration options and to optimize the compilation of the driver.
  - *freemaster\_defcfg.h* defines the default values for each FreeMASTER configuration option if the option is not set in the *freemaster\_cfg.h* file.
  - freemaster\_protocol.h defines the FreeMASTER protocol constants used internally by the driver.
  - freemaster\_protocol.c implements the FreeMASTER protocol decoder and handles the basic Get Configuration Value, Memory Read, and Memory Write commands.
  - freemaster\_rec.c handles the Recorder-specific commands and implements the Recorder sampling and triggering routines. When the Recorder is disabled by the FreeMASTER driver configuration file, this file only compiles to empty API functions.
  - *freemaster\_scope.c* handles the Oscilloscope-specific commands. If the Oscilloscope is disabled by the FreeMASTER driver configuration file, this file compiles as void.
  - *freemaster\_pipes.c* implements the Pipes functionality when the Pipes feature is enabled.
  - freemaster\_appcmd.c handles the communication commands used to deliver and execute the Application Commands within the context of the embedded application. When the Application Commands are disabled by the FreeMASTER driver configuration file, this file only compiles to empty API functions.

- freemaster\_tsa.c handles the commands specific to the TSA feature. This feature enables the FreeMASTER host tool to obtain the TSA memory descriptors declared in the embedded application. If the TSA is disabled by the FreeMASTER driver configuration file, this file compiles as void.
- freemaster\_tsa.h contains the declaration of the macros used to define the TSA memory descriptors. This file is indirectly included into the user application code (via freemaster.h).
- freemaster\_sha.c implements the SHA-1 hash code used in the password authentication algorithm.
- freemaster\_private.h contains the declarations of functions and data types used internally in the driver. It also contains the C pre-processor statements to perform the compile-time verification of the user configuration provided in the freemaster\_cfg.h file.
- freemaster\_serial.c implements the serial protocol logic including the CRC, FIFO queuing, and other communication-related operations. This code calls the functions of the low-level communication driver indirectly via a character-oriented API exported by the specific low-level driver.
- freemaster\_serial.h defines the low-level character-oriented Serial API.
- freemaster\_can.c implements the CAN protocol logic including the CAN message preparation, signalling using the first data byte in the CAN frame, and other communication-related operations. This code calls the functions of the low-level communication driver indirectly via a message-oriented API exported by the specific lowlevel driver.
- freemaster can.h defines the low-level message-oriented CAN API.
- freemaster\_net.c implements the Network protocol transport logic including multiple session management code.
- *freemaster\_net.h* definitions related to the Network transport.
- *freemaster\_pdbdm.c* implements the packet-driven BDM communication buffer and other communication-related operations.
- freemaster\_utils.c aligned memory copy routines, circular buffer management and other utility functions
- $free master\_utils.h$  definitions related to utility code.
- src/drivers/[sdk]/serial contains the code related to the serial communication implemented using one of the supported SDK frameworks.
  - freemaster\_serial\_XXX.c and .h implement low-level access to the communication peripheral registers. Different files exist for the UART, LPUART, USART, and other kinds of Serial communication modules.
- src/drivers/[sdk]/can contains the code related to the serial communication implemented using one of the supported SDK frameworks.
  - freemaster\_XXX.c and .h implement low-level access to the communication peripheral registers. Different files exist for the FlexCAN, msCAN, MCAN, and other kinds of CAN communication modules.
- *src/drivers/[sdk]/network* contains low-level code adapting the FreeMASTER Network transport to an underlying TCP/IP or RTT stack.
  - freemaster\_net\_lwip\_tcp.c and \_udp.c default networking implementation of TCP and UDP transports using lwIP stack.
  - freemaster\_net\_segger\_rtt.c implementation of network transport using Segger J-Link
     RTT interface

**Driver configuration** The driver is configured using a single header file (*freemaster\_cfg.h*). Create this file and save it together with other project source files before compiling the driver code. All FreeMASTER driver source files include the *freemaster\_cfg.h* file and use the macros defined here for the conditional and parameterized compilation. The C compiler must locate the configuration file when compiling the driver files. Typically, it can be achieved by putting this file into a folder where the other project-specific included files are stored.

As a starting point to create the configuration file, get the *freemaster\_cfg.h.example* file, rename it to *freemaster\_cfg.h*, and save it into the project area.

**Note:** It is NOT recommended to leave the *freemaster\_cfg.h* file in the FreeMASTER driver source code folder. The configuration file must be placed at a project-specific location, so that it does not affect the other applications that use the same driver.

**Configurable items** This section describes the configuration options which can be defined in *freemaster\_cfg.h*.

# **Interrupt modes**

```
#define FMSTR_LONG_INTR [0|1]
#define FMSTR_SHORT_INTR [0|1]
#define FMSTR_POLL_DRIVEN [0|1]
```

Value Type boolean (0 or 1)

**Description** Exactly one of the three macros must be defined to non-zero. The others must be defined to zero or left undefined. The non-zero-defined constant selects the interrupt mode of the driver. See *Driver interrupt modes*.

- FMSTR\_LONG\_INTR long interrupt mode
- FMSTR\_SHORT\_INTR short interrupt mode
- FMSTR\_POLL\_DRIVEN poll-driven mode

**Note:** Some options may not be supported by all communication interfaces. For example, the FMSTR\_SHORT\_INTR option is not supported by the USB\_CDC interface.

# **Protocol transport**

```
#define FMSTR_TRANSPORT [identifier]
```

**Value Type** Driver identifiers are structure instance names defined in FreeMASTER source code. Specify one of existing instances to make use of the protocol transport.

**Description** Use one of the pre-defined constants, as implemented by the FreeMASTER code. The current driver supports the following transports:

- FMSTR\_SERIAL serial communication protocol
- FMSTR CAN using CAN communication
- FMSTR\_PDBDM using packet-driven BDM communication
- FMSTR\_NET network communication using TCP or UDP protocol

**Serial transport** This section describes configuration parameters used when serial transport is used:

#define FMSTR TRANSPORT FMSTR SERIAL

**FMSTR\_SERIAL\_DRV** Select what low-level driver interface will be used when implementing the Serial communication.

#define FMSTR\_SERIAL\_DRV [identifier]

**Value Type** Driver identifiers are structure instance names defined in FreeMASTER drivers code. Specify one of existing serial driver instances.

**Description** When using MCUXpresso SDK, use one of the following constants (see /drivers/mcuxsdk/serial implementation):

- FMSTR\_SERIAL\_MCUX\_UART UART driver
- FMSTR\_SERIAL\_MCUX\_LPUART LPUART driver
- FMSTR\_SERIAL\_MCUX\_USART USART driver
- FMSTR\_SERIAL\_MCUX\_MINIUSART miniUSART driver
- FMSTR\_SERIAL\_MCUX\_QSCI DSC QSCI driver
- FMSTR\_SERIAL\_MCUX\_USB USB/CDC class driver (also see code in the /sup-port/mcuxsdk\_usb folder)
- FMSTR\_SERIAL\_56F800E\_EONCE DSC JTAG EOnCE driver

Other SDKs or BSPs may define custom low-level driver interface structure which may be used as FMSTR\_SERIAL\_DRV. For example:

• FMSTR\_SERIAL\_DREG\_UART - demonstrates the low-level interface implemented without the MCUXpresso SDK and using direct access to peripheral registers.

# **FMSTR SERIAL BASE**

#define FMSTR\_SERIAL\_BASE [address|symbol]

Value Type Optional address value (numeric or symbolic)

**Description** Specify the base address of the UART, LPUART, USART, or other serial peripheral module to be used for the communication. This value is not defined by default. User application should call FMSTR\_SetSerialBaseAddress() to select the peripheral module.

# FMSTR\_COMM\_BUFFER\_SIZE

 $\# define\ FMSTR\_COMM\_BUFFER\_SIZE\ [number]$ 

Value Type 0 or a value in range 32...255

**Description** Specify the size of the communication buffer to be allocated by the driver. Default value, which suits all driver features, is used when this option is defined as 0.

## FMSTR\_COMM\_RQUEUE\_SIZE

#define FMSTR COMM RQUEUE SIZE [number]

**Value Type** Value in range 0...255

**Description** Specify the size of the FIFO receiver queue used to quickly receive and store characters in the FMSTR\_SHORT\_INTR interrupt mode. The default value is 32 B.

# FMSTR SERIAL SINGLEWIRE

#define FMSTR\_SERIAL\_SINGLEWIRE [0|1]

**Value Type** Boolean 0 or 1.

**Description** Set to non-zero to enable the "True" single-wire mode which uses a single MCU pin to communicate. The low-level driver enables the pin direction switching when the MCU peripheral supports it.

**CAN Bus transport** This section describes configuration parameters used when CAN transport is used:

#define FMSTR\_TRANSPORT FMSTR\_CAN

**FMSTR\_CAN\_DRV** Select what low-level driver interface will be used when implementing the CAN communication.

#define FMSTR\_CAN\_DRV [identifier]

**Value Type** Driver identifiers are structure instance names defined in FreeMASTER drivers code. Specify one of existing CAN driver instances.

**Description** When using MCUXpresso SDK, use one of the following constants (see /drivers/mcuxsdk/can implementation):

- FMSTR\_CAN\_MCUX\_FLEXCAN FlexCAN driver
- FMSTR\_CAN\_MCUX\_MCAN MCAN driver
- FMSTR\_CAN\_MCUX\_MSCAN msCAN driver
- FMSTR\_CAN\_MCUX\_DSCFLEXCAN DSC FlexCAN driver
- FMSTR CAN MCUX DSCMSCAN DSC msCAN driver

Other SDKs or BSPs may define the custom low-level driver interface structure which may be used as FMSTR\_CAN\_DRV.

FMSTR\_CAN\_BASE

#define FMSTR\_CAN\_BASE [address|symbol]

**Value Type** Optional address value (numeric or symbolic)

**Description** Specify the base address of the FlexCAN, msCAN, or other CAN peripheral module to be used for the communication. This value is not defined by default. User application should call FMSTR\_SetCanBaseAddress() to select the peripheral module.

#### **FMSTR CAN CMDID**

#define FMSTR\_CAN\_CMDID [number]

Value Type CAN identifier (11-bit or 29-bit number)

**Description** CAN message identifier used for FreeMASTER commands (direction from PC Host tool to target application). When declaring 29-bit identifier, combine the numeric value with FMSTR\_CAN\_EXTID bit. Default value is 0x7AA.

# FMSTR\_CAN\_RSPID

#define FMSTR\_CAN\_RSPID [number]

**Value Type** CAN identifier (11-bit or 29-bit number)

**Description** CAN message identifier used for responding messages (direction from target application to PC Host tool). When declaring 29-bit identifier, combine the numeric value with FMSTR\_CAN\_EXTID bit. Note that both *CMDID* and *RSPID* values may be the same. Default value is 0x7AA.

# FMSTR\_FLEXCAN\_TXMB

#define FMSTR\_FLEXCAN\_TXMB [number]

**Value Type** Number in range of 0..N where N is number of CAN message-buffers supported by HW module.

**Description** Only used when the FlexCAN low-level driver is used. Define the FlexCAN message buffer for CAN frame transmission. Default value is 0.

## FMSTR\_FLEXCAN\_RXMB

#define FMSTR\_FLEXCAN\_RXMB [number]

**Value Type** Number in range of 0..N where N is number of CAN message-buffers supported by HW module.

**Description** Only used when the FlexCAN low-level driver is used. Define the FlexCAN message buffer for CAN frame reception. Note that the FreeMASTER driver may also operate with a common message buffer used by both TX and RX directions. Default value is 1.

**Network transport** This section describes configuration parameters used when Network transport is used:

#define FMSTR\_TRANSPORT FMSTR\_NET

FMSTR NET DRV Select network interface implementation.

#define FMSTR\_NET\_DRV [identifier]

**Value Type** Identifiers are structure instance names defined in FreeMASTER drivers code. Specify one of existing NET driver instances.

**Description** When using MCUXpresso SDK, use one of the following constants (see /drivers/mcuxsdk/network implementation):

- FMSTR\_NET\_LWIP\_TCP TCP communication using lwIP stack
- FMSTR\_NET\_LWIP\_UDP UDP communication using lwIP stack
- FMSTR\_NET\_SEGGER\_RTT Communication using SEGGER J-Link RTT interface

Other SDKs or BSPs may define the custom networking interface which may be used as FM-STR CAN DRV.

Add another row below:

# **FMSTR NET PORT**

#define FMSTR\_NET\_PORT [number]

**Value Type** TCP or UDP port number (short integer)

**Description** Specifies the server port number used by TCP or UDP protocols.

# FMSTR\_NET\_BLOCKING\_TIMEOUT

#define FMSTR\_NET\_BLOCKING\_TIMEOUT [number]

Value Type Timeout as number of milliseconds

**Description** This value specifies a timeout in milliseconds for which the network socket operations may block the execution inside *FMSTR\_Poll*. This may be set high (e.g. 250) when a dedicated RTOS task is used to handle FreeMASTER protocol polling. Set to a lower value when the polling task is also responsible for other operations. Set to 0 to attempt to use non-blocking socket operations.

#### FMSTR\_NET\_AUTODISCOVERY

#define FMSTR\_NET\_AUTODISCOVERY [0|1]

**Value Type** Boolean 0 or 1.

**Description** This option enables the FreeMASTER driver to use a separate UDP socket to broadcast auto-discovery messages to network. This helps the FreeMASTER tool to discover the target device address, port and protocol options.

**Debugging options** 

## FMSTR\_DISABLE

#define FMSTR\_DISABLE [0|1]

Value Type boolean (0 or 1)

**Description** Define as non-zero to disable all FreeMASTER features, exclude the driver code from build, and compile all its API functions empty. This may be useful to remove FreeMASTER without modifying any application source code. Default value is 0 (false).

# **FMSTR DEBUG TX**

#define FMSTR\_DEBUG\_TX [0|1]

**Value Type** Boolean 0 or 1.

**Description** Define as non-zero to enable the driver to periodically transmit test frames out on the selected communication interface (SCI or CAN). With the debug transmission enabled, it is simpler to detect problems in the baudrate or other communication configuration settings.

The test frames are transmitted until the first valid command frame is received from the PC Host tool. The test frame is a valid error status frame, as defined by the protocol format. On the serial line, the test frame consists of three printable characters (+©W) which are easy to capture using the serial terminal tools.

This feature requires the FMSTR\_Poll() function to be called periodically. Default value is 0 (false).

## FMSTR\_APPLICATION\_STR

#define FMSTR\_APPLICATION\_STR

Value Type String.

**Description** Name of the application visible in FreeMASTER host application.

**Memory access** 

# FMSTR\_USE\_READMEM

#define FMSTR\_USE\_READMEM [0|1]

Value Type Boolean 0 or 1.

**Description** Define as non-zero to implement the Memory Read command and enable FreeMASTER to have read access to memory and variables. The access can be further restricted by using a TSA feature.

Default value is 1 (true).

# **FMSTR USE WRITEMEM**

#define FMSTR\_USE\_WRITEMEM [0|1]

Value Type Boolean 0 or 1.

**Description** Define as non-zero to implement the Memory Write command. The default value is 1 (true).

# Oscilloscope options

# FMSTR\_USE\_SCOPE

#define FMSTR\_USE\_SCOPE [number]

Value Type Integer number.

**Description** Number of Oscilloscope instances to be supported. Set to 0 to disable the Oscilloscope feature.

Default value is 0.

# FMSTR\_MAX\_SCOPE\_VARS

#define FMSTR\_MAX\_SCOPE\_VARS [number]

Value Type Integer number larger than 2.

**Description** Number of variables to be supported by each Oscilloscope instance. Default value is 8.

# **Recorder options**

# FMSTR\_USE\_RECORDER

#define FMSTR\_USE\_RECORDER [number]

Value Type Integer number.

**Description** Number of Recorder instances to be supported. Set to 0 to disable the Recorder feature.

Default value is 0.

# FMSTR\_REC\_BUFF\_SIZE

```
#define FMSTR_REC_BUFF_SIZE [number]
```

Value Type Integer number larger than 2.

**Description** Defines the size of the memory buffer used by the Recorder instance #0. Default: not defined, user shall call 'FMSTR\_RecorderCreate()" API function to specify this parameter in run time.

#### FMSTR REC TIMEBASE

```
#define FMSTR_REC_TIMEBASE [time specification]
```

Value Type Number (nanoseconds time).

**Description** Defines the base sampling rate in nanoseconds (sampling speed) Recorder instance #0.

Use one of the following macros:

- FMSTR\_REC\_BASE\_SECONDS(x)
- FMSTR\_REC\_BASE\_MILLISEC(x)
- FMSTR\_REC\_BASE\_MICROSEC(x)
- FMSTR\_REC\_BASE\_NANOSEC(x)

Default: not defined, user shall call 'FMSTR\_RecorderCreate()" API function to specify this parameter in run time.

## FMSTR REC FLOAT TRIG

```
#define FMSTR_REC_FLOAT_TRIG [0|1]
```

**Value Type** Boolean 0 or 1.

**Description** Define as non-zero to implement the floating-point triggering. Be aware that floating-point triggering may grow the code size by linking the floating-point standard library. Default value is 0 (false).

# **Application Commands options**

#### FMSTR\_USE\_APPCMD

#define FMSTR\_USE\_APPCMD [0|1]

**Value Type** Boolean 0 or 1.

**Description** Define as non-zero to implement the Application Commands feature. Default value is 0 (false).

# FMSTR APPCMD BUFF SIZE

#define FMSTR\_APPCMD\_BUFF\_SIZE [size]

**Value Type** Numeric buffer size in range 1..255

**Description** The size of the Application Command data buffer allocated by the driver. The buffer stores the (optional) parameters of the Application Command which waits to be processed.

# FMSTR\_MAX\_APPCMD\_CALLS

#define FMSTR\_MAX\_APPCMD\_CALLS [number]

**Value Type** Number in range 0..255

**Description** The number of different Application Commands that can be assigned a callback handler function using  $FMSTR\_RegisterAppCmdCall()$ . Default value is 0.

**TSA options** 

### FMSTR\_USE\_TSA

#define FMSTR USE TSA [0|1]

Value Type Boolean 0 or 1.

**Description** Enable the FreeMASTER TSA feature to be used. With this option enabled, the TSA tables defined in the applications are made available to the FreeMASTER host tool. Default value is 0 (false).

# FMSTR\_USE\_TSA\_SAFETY

#define FMSTR\_USE\_TSA\_SAFETY [0|1]

Value Type Boolean 0 or 1.

**Description** Enable the memory access validation in the FreeMASTER driver. With this option, the host tool is not able to access the memory which is not described by at least one TSA descriptor. Also a write access is denied for objects defined as read-only in TSA tables. Default value is 0 (false).

# FMSTR\_USE\_TSA\_INROM

#define FMSTR\_USE\_TSA\_INROM [0|1]

**Value Type** Boolean 0 or 1.

**Description** Declare all TSA descriptors as *const*, which enables the linker to put the data into the flash memory. The actual result depends on linker settings or the linker commands used in the project.

Default value is 0 (false).

#### FMSTR USE TSA DYNAMIC

#define FMSTR\_USE\_TSA\_DYNAMIC [0|1]

**Value Type** Boolean 0 or 1.

**Description** Enable runtime-defined TSA entries to be added to the TSA table by the  ${
m FM-STR\_SetUpTsaBuff()}$  and  ${
m FMSTR\_TsaAddVar()}$  functions. Default value is 0 (false).

# **Pipes options**

#### FMSTR\_USE\_PIPES

#define FMSTR USE PIPES [0|1]

Value Type Boolean 0 or 1.

**Description** Enable the FreeMASTER Pipes feature to be used. Default value is 0 (false).

# FMSTR MAX PIPES COUNT

#define FMSTR\_MAX\_PIPES\_COUNT [number]

**Value Type** Number in range 1..63.

**Description** The number of simultaneous pipe connections to support. The default value is 1.

**Driver interrupt modes** To implement the communication, the FreeMASTER driver handles the Serial or CAN module's receive and transmit requests. Use the *freemaster\_cfg.h* configuration file to select whether the driver processes the communication automatically in the interrupt service routine handler or if it only polls the status of the module (typically during the application idle time).

This section describes each of the interrupt mode in more details.

# **Completely Interrupt-Driven operation** Activated using:

```
#define FMSTR_LONG_INTR 1
```

In this mode, both the communication and the FreeMASTER protocol decoding is done in the *FMSTR\_SerialIsr*, *FMSTR\_CanIsr*, or other interrupt service routine. Because the protocol execution may be a lengthy task (especially with the TSA-Safety enabled) it is recommended to use this mode only if the interrupt prioritization scheme is possible in the application and the FreeMASTER interrupt is assigned to a lower (the lowest) priority.

In this mode, the application code must register its own interrupt handler for all interrupt vectors related to the selected communication interface and call the FMSTR\_SerialIsr or FMSTR\_CanIsr functions from that handler.

# Mixed Interrupt and Polling Modes Activated using:

```
#define FMSTR SHORT INTR 1
```

In this mode, the communication processing time is split between the interrupt routine and the main application loop or task. The raw communication is handled by the <code>FMSTR\_SerialIsr</code>, <code>FM-STR\_CanIsr</code>, or other interrupt service routine, while the protocol decoding and execution is handled by the <code>FMSTR\_Poll</code> routine. Call <code>FMSTR\_Poll</code> during the idle time in the application main loop.

The interrupt processing in this mode is relatively fast and deterministic. Upon a serial-receive event, the received character is only placed into a FIFO-like queue and it is not further processed. Upon a CAN receive event, the received frame is stored into a receive buffer. When transmitting, the characters are fetched from the prepared transmit buffer.

In this mode, the application code must register its own interrupt handler for all interrupt vectors related to the selected communication interface and call the *FMSTR\_SerialIsr* or *FM-STR\_CanIsr* functions from that handler.

When the serial interface is used as the serial communication interface, ensure that the FM- $STR\_Poll$  function is called at least once per N character time periods. N is the length of the FreeMASTER FIFO queue ( $FMSTR\_COMM\_RQUEUE\_SIZE$ ) and the character time is the time needed to transmit or receive a single byte over the SCI line.

# **Completely Poll-driven**

```
#define FMSTR_POLL_DRIVEN 1
```

In this mode, both the communication and the FreeMASTER protocol decoding are done in the *FMSTR\_Poll* routine. No interrupts are needed and the *FMSTR\_SerialIsr*, *FMSTR\_CanIsr*, and similar handlers compile to an empty code.

When using this mode, ensure that the *FMSTR\_Poll* function is called by the application at least once per the serial "character time" which is the time needed to transmit or receive a single character.

In the latter two modes (FMSTR\_SHORT\_INTR and FMSTR\_POLL\_DRIVEN), the protocol handling takes place in the FMSTR\_Poll routine. An application interrupt can occur in the middle of the

Read Memory or Write Memory commands' execution and corrupt the variable being accessed by the FreeMASTER driver. In these two modes, some issues or glitches may occur when using FreeMASTER to visualize or monitor volatile variables modified in interrupt servicing code.

The same issue may appear even in the full interrupt mode (FMSTR\_LONG\_INTR), if volatile variables are modified in the interrupt code with a priority higher than the priority of the communication interrupt.

**Data types** Simple portability was one of the main requirements when writing the FreeMAS-TER driver. This is why the driver code uses the privately-declared data types and the vast majority of the platform-dependent code is separated in the platform-dependent source files. The data types used in the driver API are all defined in the platform-specific header file.

To prevent name conflicts with the symbols used in the application, all data types, macros, and functions have the FMSTR\_prefix. The only global variables used in the driver are the transport and low-level API structures exported from the driver-implementation layer to upper layers. Other than that, all private variables are declared as static and named using the fmstr\_prefix.

**Communication interface initialization** The FreeMASTER driver does not perform neither the initialization nor the configuration of the peripheral module that it uses to communicate. It is the application startup code responsibility to configure the communication module before the FreeMASTER driver is initialized by the FMSTR\_Init call.

When the Serial communication module is used as the FreeMASTER communication interface, configure the UART receive and transmit pins, the serial communication baud rate, parity (noparity), the character length (eight bits), and the number of stop bits (one) before initializing the FreeMASTER driver. For either the long or the short interrupt modes of the driver (see *Driver interrupt modes*), configure the interrupt controller and register an application-specific interrupt handler for all interrupt sources related to the selected serial peripheral module. Call the FMSTR\_SerialIsr function from the application handler.

When a CAN module is used as the FreeMASTER communication interface, configure the CAN receive and transmit pins and the CAN module bit rate before initializing the FreeMASTER driver. For either the long or the short interrupt modes of the driver (see *Driver interrupt modes*), configure the interrupt controller and register an application-specific interrupt handler for all interrupt sources related to the selected CAN peripheral module. Call the FMSTR\_CanIsr function from the application handler.

**Note:** It is not necessary to enable or unmask the serial nor the CAN interrupts before initializing the FreeMASTER driver. The driver enables or disables the interrupts and communication lines, as required during runtime.

FreeMASTER Recorder calls When using the FreeMASTER Recorder in the application (FM-STR\_USE\_RECORDER > 0), call the FMSTR\_RecorderCreate function early after FMSTR\_Init to set up each recorder instance to be used in the application. Then call the FMSTR\_Recorder function periodically in the code where the data recording should occur. A typical place to call the Recorder routine is at the timer or PWM interrupts, but it can be anywhere else. The example applications provided together with the driver code call the FMSTR\_Recorder in the main application loop.

In applications where FMSTR\_Recorder is called periodically with a constant period, specify the period in the Recorder configuration structure before calling FMSTR\_RecorderCreate. This setting enables the PC Host FreeMASTER tool to display the X-axis of the Recorder graph properly scaled for the time domain.

**Driver usage** Start using or evaluating FreeMASTER by opening some of the example applications available in the driver setup package.

Follow these steps to enable the basic FreeMASTER connectivity in the application:

- Make sure that all \*c files of the FreeMASTER driver from the src/common/platforms/[your\_platform] folder are a part of the project. See Driver files for more details.
- Configure the FreeMASTER driver by creating or editing the *freemaster\_cfg.h* file and by saving it into the application project directory. See *Driver configuration* for more details.
- Include the *freemaster.h* file into any application source file that makes the FreeMASTER API calls.
- Initialize the Serial or CAN modules. Set the baud rate, parity, and other parameters of the communication. Do not enable the communication interrupts in the interrupt mask registers.
- For the FMSTR\_LONG\_INTR and FMSTR\_SHORT\_INTR modes, install the application-specific interrupt routine and call the FMSTR\_SerialIsr or FMSTR\_CanIsr functions from this handler.
- Call the FMSTR\_Init function early on in the application initialization code.
- Call the FMSTR\_RecorderCreate functions for each Recorder instance to enable the Recorder feature.
- In the main application loop, call the FMSTR\_Poll API function periodically when the application is idle.
- For the FMSTR\_SHORT\_INTR and FMSTR\_LONG\_INTR modes, enable the interrupts globally so that the interrupts can be handled by the CPU.

**Communication troubleshooting** The most common problem that causes communication issues is a wrong baud rate setting or a wrong pin multiplexer setting of the target MCU. When a communication between the PC Host running FreeMASTER and the target MCU cannot be established, try enabling the FMSTR\_DEBUG\_TX option in the *freemaster\_cfg.h* file and call the FMSTR\_Poll function periodically in the main application task loop.

With this feature enabled, the FreeMASTER driver periodically transmits a test frame through the Serial or CAN lines. Use a logic analyzer or an oscilloscope to monitor the signals at the communication pins of the CPU device to examine whether the bit rate and signal polarity are configured properly.

#### **Driver API**

This section describes the driver Application Programmers' Interface (API) needed to initialize and use the FreeMASTER serial communication driver.

**Control API** There are three key functions to initialize and use the driver.

#### **FMSTR Init**

## **Prototype**

FMSTR\_BOOL FMSTR\_Init(void);

- Declaration: freemaster.h
- Implementation: freemaster protocol.c

**Description** This function initializes the internal variables of the FreeMASTER driver and enables the communication interface. This function does not change the configuration of the selected communication module. The hardware module must be initialized before the *FMSTR\_Init* function is called.

A call to this function must occur before calling any other FreeMASTER driver API functions.

#### FMSTR\_Poll

## **Prototype**

```
void FMSTR_Poll(void);
```

• Declaration: freemaster.h

• Implementation: freemaster\_protocol.c

**Description** In the poll-driven or short interrupt modes, this function handles the protocol decoding and execution (see *Driver interrupt modes*). In the poll-driven mode, this function also handles the communication interface with the PC. Typically, the *FMSTR\_Poll* function is called during the "idle" time in the main application task loop.

To prevent the receive data overflow (loss) on a serial interface, make sure that the FMSTR\_Poll function is called at least once per the time calculated as:

N \* Tchar

#### where:

- *N* is equal to the length of the receive FIFO queue (configured by the FM-STR\_COMM\_RQUEUE\_SIZE macro). *N* is 1 for the poll-driven mode.
- *Tchar* is the character time, which is the time needed to transmit or receive a single byte over the SCI line.

**Note:** In the long interrupt mode, this function typically compiles as an empty function and can still be called. It is worthwhile to call this function regardless of the interrupt mode used in the application. This approach enables a convenient switching between the different interrupt modes only by changing the configuration macros in the *freemaster cfg.h* file.

## FMSTR SerialIsr / FMSTR CanIsr

#### **Prototype**

```
void FMSTR_SerialIsr(void);
void FMSTR_CanIsr(void);
```

• Declaration: freemaster.h

• Implementation: hw-specific low-level driver C file

**Description** This function contains the interrupt-processing code of the FreeMASTER driver. In long or short interrupt modes (see *Driver interrupt modes*), this function must be called from the application interrupt service routine registered for the communication interrupt vector. On platforms where the communication module uses multiple interrupt vectors, the application should register a handler for all vectors and call this function at each interrupt.

**Note:** In a poll-driven mode, this function is compiled as an empty function and does not have to be used.

#### **Recorder API**

#### FMSTR\_RecorderCreate

#### **Prototype**

FMSTR\_BOOL FMSTR\_RecorderCreate(FMSTR\_INDEX recIndex, FMSTR\_REC\_BUFF\* buffCfg);

• Declaration: freemaster.h

• Implementation: freemaster\_rec.c

**Description** This function registers a recorder instance and enables it to be used by the PC Host tool. Call this function for all recorder instances from 0 to the maximum number defined by the FMSTR\_USE\_RECORDER configuration option (minus one). An exception to this requirement is the recorder of instance 0 which may be automatically configured by FMSTR\_Init when the *freemaster\_cfg.h* configuration file defines the *FMSTR\_REC\_BUFF\_SIZE* and *FMSTR\_REC\_TIMEBASE* options.

For more information, see *Configurable items*.

#### FMSTR\_Recorder

## **Prototype**

void FMSTR\_Recorder(FMSTR\_INDEX recIndex);

• Declaration: freemaster.h

• Implementation: freemaster rec.c

**Description** This function takes a sample of the variables being recorded using the FreeMAS-TER Recorder instance *recIndex*. If the selected Recorder is not active when the *FMSTR\_Recorder* function is being called, the function returns immediately. When the Recorder is active, the values of the variables being recorded are copied into the recorder buffer and the trigger conditions are evaluated.

If a trigger condition is satisfied, the Recorder enters the post-trigger mode, where it counts down the follow-up samples (number of *FMSTR\_Recorder* function calls) and de-activates the Recorder when the required post-trigger samples are finished.

The *FMSTR\_Recorder* function is typically called in the timer or PWM interrupt service routines. This function can also be called in the application main loop (for testing purposes).

#### FMSTR\_RecorderTrigger

#### **Prototype**

void FMSTR\_RecorderTrigger(FMSTR\_INDEX recIndex);

• Declaration: freemaster.h

• Implementation: *freemaster\_rec.c* 

**Description** This function forces the Recorder trigger condition to happen, which causes the Recorder to be automatically deactivated after the post-trigger samples are sampled. Use this function in the application code for programmatic control over the Recorder triggering. This can be useful when a more complex triggering conditions need to be used.

**Fast Recorder API** The Fast Recorder feature is not available in the FreeMASTER driver version 3. This feature was heavily dependent on the target platform and it was only available for the 56F8xxxx DSCs.

**TSA Tables** When the TSA is enabled in the FreeMASTER driver configuration file (by setting the FMSTR\_USE\_TSA macro to a non-zero value), it defines the so-called TSA tables in the application. This section describes the macros that must to be used to define the TSA tables.

There can be any number of TSA tables spread across the application source files. There must be always exactly one TSA Table List defined, which informs the FreeMASTER driver about the active TSA tables.

When there is at least one TSA table and one TSA Table List defined in the application, the TSA information automatically appears in the FreeMASTER symbols list. The symbols can then be used to create FreeMASTER variables for visualization or control.

**TSA table definition** The TSA table describes the static or global variables together with their address, size, type, and access-protection information. If the TSA-described variables are of a structure type, the TSA table may also describe this type and provide an access to the individual structure members of the variable.

The TSA table definition begins with the FMSTR\_TSA\_TABLE\_BEGIN macro with a *table\_id* identifying the table. The *table\_id* shall be a valid C-langiage symbol.

```
FMSTR_TSA_TABLE_BEGIN(table_id)
```

After this opening macro, the TSA descriptors are placed using these macros:

```
/* Adding variable descriptors */
FMSTR_TSA_RW_VAR(name, type) /* read/write variable entry */
FMSTR_TSA_RO_VAR(name, type) /* read-only variable entry */

/* Description of complex data types */
FMSTR_TSA_STRUCT(struct_name) /* structure or union type entry */
FMSTR_TSA_MEMBER(struct_name, member_name, type) /* structure member entry */

/* Memory blocks */
FMSTR_TSA_RW_MEM(name, type, address, size) /* read/write memory block */
FMSTR_TSA_RO_MEM(name, type, address, size) /* read-only memory block */
```

The table is closed using the FMSTR\_TSA\_TABLE\_END macro:

```
FMSTR_TSA_TABLE_END()
```

**TSA descriptor parameters** The TSA descriptor macros accept these parameters:

- name variable name. The variable must be defined before the TSA descriptor references it
- *type* variable or member type. Only one of the pre-defined type constants may be used (see below).
- *struct\_name* structure type name. The type must be defined (typedef) before the TSA descriptor references it.

• *member\_name* — structure member name.

**Note:** The structure member descriptors (FMSTR\_TSA\_MEMBER) must immediately follow the parent structure descriptor (FMSTR\_TSA\_STRUCT) in the table.

**Note:** To write-protect the variables in the FreeMASTER driver (FMSTR\_TSA\_RO\_VAR), enable the TSA-Safety feature in the configuration file.

TSA variable types	The table lists <i>type</i> identifiers v	which can be used in TSA descriptors
--------------------	---	--------------------------------------

Constant	Description
FMSTR_TSA_UINTn	Unsigned integer type of size <i>n</i> bits (n=8,16,32,64)
FMSTR_TSA_SINTn	Signed integer type of size <i>n</i> bits (n=8,16,32,64)
FMSTR_TSA_FRACn	Fractional number of size $n$ bits (n=16,32,64).
$FMSTR_TSA_FRAC_Q(m,n)$	Signed fractional number in general Q form (m+n+1 total bits)
FMSTR_TSA_FRAC_UQ(m,n)	Unsigned fractional number in general UQ form (m+n total bits)
FMSTR_TSA_FLOAT	4-byte standard IEEE floating-point type
FMSTR_TSA_DOUBLE	8-byte standard IEEE floating-point type
FMSTR_TSA_POINTER	Generic pointer type defined (platform-specific 16 or 32 bit)
FM-	Structure or union type declared with FMSTR_TSA_STRUCT
STR_TSA_USERTYPE(name)	record

**TSA table list** There shall be exactly one TSA Table List in the application. The list contains one entry for each TSA table defined anywhere in the application.

The TSA Table List begins with the FMSTR\_TSA\_TABLE\_LIST\_BEGIN macro and continues with the TSA table entries for each table.

```
FMSTR_TSA_TABLE_LIST_BEGIN()

FMSTR_TSA_TABLE(table_id)

FMSTR_TSA_TABLE(table_id2)

FMSTR_TSA_TABLE(table_id3)

...
```

The list is closed with the FMSTR\_TSA\_TABLE\_LIST\_END macro:

```
FMSTR_TSA_TABLE_LIST_END()
```

**TSA Active Content entries** FreeMASTER v2.0 and higher supports TSA Active Content, enabling the TSA tables to describe the memory-mapped files, virtual directories, and URL hyperlinks. FreeMASTER can access such objects similarly to accessing the files and folders on the local hard drive.

With this set of TSA entries, the FreeMASTER pages can be embedded directly into the target MCU flash and accessed by FreeMASTER directly over the communication line. The HTML-coded pages rendered inside the FreeMASTER window can access the TSA Active Content resources using a special URL referencing the *fmstr*: protocol.

This example provides an overview of the supported TSA Active Content entries:

```
FMSTR_TSA_TABLE_BEGIN(files_and_links)

/* Directory entry applies to all subsequent MEMFILE entries */
FMSTR_TSA_DIRECTORY("/text_files") /* entering a new virtual directory */

(continues on next page)
```

(continued from previous page)

```
/* The readme.txt file will be accessible at the fmstr://text_files/readme.txt URL */
FMSTR_TSA_MEMFILE("readme.txt", readme_txt, sizeof(readme_txt)) /* memory-mapped file */

/* Files can also be specified with a full path so the DIRECTORY entry does not apply */
FMSTR_TSA_MEMFILE("/index.htm", index, sizeof(index)) /* memory-mapped file */
FMSTR_TSA_MEMFILE("/prj/demo.pmp", demo_pmp, sizeof(demo_pmp)) /* memory-mapped file */

/* Hyperlinks can point to a local MEMFILE object or to the Internet */
FMSTR_TSA_HREF("Board's Built-in Welcome Page", "/index.htm")
FMSTR_TSA_HREF("FreeMASTER Home Page", "http://www.nxp.com/freemaster")

/* Project file links simplify opening the projects from any URLs */
FMSTR_TSA_PROJECT("Demonstration Project (embedded)", "/prj/demo.pmp")
FMSTR_TSA_PROJECT("Full Project (online)", "http://mycompany.com/prj/demo.pmp")
FMSTR_TSA_TABLE_END()
```

#### TSA API

#### FMSTR\_SetUpTsaBuff

## **Prototype**

FMSTR\_BOOL FMSTR\_SetUpTsaBuff(FMSTR\_ADDR buffAddr, FMSTR\_SIZE buffSize);

- Declaration: freemaster.h
- Implementation: freemaster tsa.c

#### Arguments

- buffAddr [in] address of the memory buffer for the dynamic TSA table
- *buffSize* [in] size of the memory buffer which determines the maximum number of TSA entries to be added in the runtime

**Description** This function must be used to assign the RAM memory buffer to the TSA subsystem when FMSTR\_USE\_TSA\_DYNAMIC is enabled. The memory buffer is then used to store the TSA entries added dynamically to the runtime TSA table using the FMSTR\_TsaAddVar function call. The runtime TSA table is processed by the FreeMASTER PC Host tool along with all static tables as soon as the communication port is open.

The size of the memory buffer determines the number of TSA entries that can be added dynamically. Depending on the MCU platform, one TSA entry takes either 8 or 16 bytes.

#### FMSTR\_TsaAddVar

#### **Prototype**

```
FMSTR\_BOOL\ FMSTR\_TsaAddVar(FMSTR\_TSATBL\_STRPTR\ tsaName,\ FMSTR\_TSATBL\_STRPTR_{\ }\ tsaType,\\ FMSTR\_TSATBL\_VOIDPTR\ varAddr,\ FMSTR\_SIZE32\ varSize,\\ FMSTR\_SIZE\ flags);
```

• Declaration: freemaster.h

• Implementation: freemaster\_tsa.c

## **Arguments**

- tsaName [in] name of the object
- tsaType [in] name of the object type
- varAddr [in] address of the object
- *varSize* [in] size of the object
- flags [in] access flags; a combination of these values:
  - FMSTR\_TSA\_INFO\_RO\_VAR read-only memory-mapped object (typically a variable)
  - FMSTR\_TSA\_INFO\_RW\_VAR read/write memory-mapped object
  - *FMSTR\_TSA\_INFO\_NON\_VAR* other entry, describing structure types, structure members, enumerations, and other types

**Description** This function can be called only when the dynamic TSA table is enabled by the FMSTR\_USE\_TSA\_DYNAMIC configuration option and when the FMSTR\_SetUpTsaBuff function call is made to assign the dynamic TSA table memory. This function adds an entry into the dynamic TSA table. It can be used to register a read-only or read/write memory object or describe an item of the user-defined type.

See TSA table definition for more details about the TSA table entries.

## **Application Commands API**

#### FMSTR\_GetAppCmd

#### **Prototype**

#### FMSTR\_APPCMD\_CODE FMSTR\_GetAppCmd(void);

- Declaration: freemaster.h
- Implementation: freemaster\_appcmd.c

**Description** This function can be used to detect if there is an Application Command waiting to be processed by the application. If no command is pending, this function returns the FM-STR\_APPCMDRESULT\_NOCMD constant. Otherwise, this function returns the code of the Application Command that must be processed. Use the FMSTR\_AppCmdAck call to acknowledge the Application Command after it is processed and to return the appropriate result code to the host.

The FMSTR\_GetAppCmd function does not report the commands for which a callback handler function exists. If the FMSTR\_GetAppCmd function is called when a callback-registered command is pending (and before it is actually processed by the callback function), this function returns FMSTR\_APPCMDRESULT\_NOCMD.

#### FMSTR\_GetAppCmdData

#### **Prototype**

FMSTR APPCMD PDATA FMSTR GetAppCmdData(FMSTR SIZE\* dataLen);

• Declaration: freemaster.h

• Implementation: freemaster\_appcmd.c

## **Arguments**

• *dataLen* [out] - pointer to the variable that receives the length of the data available in the buffer. It can be NULL when this information is not needed.

**Description** This function can be used to retrieve the Application Command data when the application determines that an Application Command is pending (see *FMSTR\_GetAppCmd*).

There is just a single buffer to hold the Application Command data (the buffer length is FM-STR\_APPCMD\_BUFF\_SIZE bytes). If the data are to be used in the application after the command is processed by the FMSTR\_AppCmdAck call, copy the data out to a private buffer.

## FMSTR\_AppCmdAck

## **Prototype**

void FMSTR\_AppCmdAck(FMSTR\_APPCMD\_RESULT resultCode);

• Declaration: freemaster.h

• Implementation: freemaster\_appcmd.c

## **Arguments**

• resultCode [in] - the result code which is to be returned to FreeMASTER

**Description** This function is used when the Application Command processing finishes in the application. The resultCode passed to this function is returned back to the host and the driver is re-initialized to expect the next Application Command.

After this function is called and before the next Application Command arrives, the return value of the FMSTR\_GetAppCmd function is FMSTR\_APPCMDRESULT\_NOCMD.

## FMSTR\_AppCmdSetResponseData

#### **Prototype**

void FMSTR\_AppCmdSetResponseData(FMSTR\_ADDR resultDataAddr, FMSTR\_SIZE resultDataLen);

• Declaration: freemaster.h

• Implementation: freemaster\_appcmd.c

#### **Arguments**

- resultDataAddr [in] pointer to the data buffer that is to be copied to the Application Command data buffer
- resultDataLen [in] length of the data to be copied. It must not exceed the FM-STR APPCMD BUFF SIZE value.

**Description** This function can be used before the Application Command processing finishes, when there are data to be returned back to the PC.

The response data buffer is copied into the Application Command data buffer, from where it is accessed when the host requires it. Do not use FMSTR\_GetAppCmdData and the data buffer after FMSTR\_AppCmdSetResponseData is called.

**Note:** The current version of FreeMASTER does not support the Application Command response data.

## FMSTR\_RegisterAppCmdCall

## **Prototype**

FMSTR\_BOOL FMSTR\_RegisterAppCmdCall(FMSTR\_APPCMD\_CODE appCmdCode, FMSTR\_ --PAPPCMDFUNC callbackFunc);

- Declaration: freemaster.h
- Implementation: freemaster\_appcmd.c

#### **Arguments**

- appCmdCode [in] the Application Command code for which the callback is to be registered
- *callbackFunc* [in] pointer to the callback function that is to be registered. Use NULL to unregister a callback registered previously with this Application Command.

**Return value** This function returns a non-zero value when the callback function was successfully registered or unregistered. It can return zero when trying to register a callback function for more than FMSTR\_MAX\_APPCMD\_CALLS different Application Commands.

**Description** This function can be used to register the given function as a callback handler for the Application Command. The Application Command is identified using single-byte code. The callback function is invoked automatically by the FreeMASTER driver when the protocol decoder obtains a request to get the application command result code.

The prototype of the callback function is

FMSTR\_APPCMD\_RESULT HandlerFunction(FMSTR\_APPCMD\_CODE nAppcmd, FMSTR\_APPCMD\_PDATA pData, FMSTR\_SIZE nDataLen);

#### Where:

- nAppcmd -Application Command code
- pData —points to the Application Command data received (if any)
- *nDataLen* —information about the Application Command data length

The return value of the callback function is used as the Application Command Result Code and returned to FreeMASTER.

**Note:** The FMSTR\_MAX\_APPCMD\_CALLS configuration macro defines how many different Application Commands may be handled by a callback function. When FMSTR\_MAX\_APPCMD\_CALLS is undefined or defined as zero, the FMSTR\_RegisterAppCmdCall function always fails.

## **Pipes API**

## FMSTR\_PipeOpen

## **Prototype**

```
FMSTR_HPIPE FMSTR_PipeOpen(FMSTR_PIPE_PORT pipePort, FMSTR_PPIPEFUNC pipeCallback,

FMSTR_ADDR pipeRxBuff, FMSTR_PIPE_SIZE pipeRxSize,
FMSTR_ADDR pipeTxBuff, FMSTR_PIPE_SIZE pipeTxSize,
FMSTR_U8 type, const FMSTR_CHAR *name);
```

- Declaration: freemaster.h
- Implementation: freemaster\_pipes.c

## **Arguments**

- pipePort [in] port number that identifies the pipe for the client
- pipeCallback [in] pointer to the callback function that is called whenever a pipe data status changes
- pipeRxBuff [in] address of the receive memory buffer
- pipeRxSize [in] size of the receive memory buffer
- pipeTxBuff [in] address of the transmit memory buffer
- pipeTxSize [in] size of the transmit memory buffer
- *type* [in] a combination of FMSTR\_PIPE\_MODE\_xxx and FMSTR\_PIPE\_SIZE\_xxx constants describing primary pipe data format and usage. This type helps FreeMASTER decide how to access the pipe by default. Optional, use 0 when undetermined.
- *name* [in] user name of the pipe port. This name is visible to the FreeMASTER user when creating the graphical pipe interface.

**Description** This function initializes a new pipe and makes it ready to accept or send the data to the PC Host client. The receive memory buffer is used to store the received data before they are read out by the FMSTR\_PipeRead call. When this buffer gets full, the PC Host client denies the data transmission into this pipe until there is enough free space again. The transmit memory buffer is used to store the data transmitted by the application to the PC Host client using the FMSTR\_PipeWrite call. The transmit buffer can get full when the PC Host is disconnected or when it is slow in receiving and reading out the pipe data.

The function returns the pipe handle which must be stored and used in the subsequent calls to manage the pipe object.

The callback function (if specified) is called whenever new data are received through the pipe and available for reading. This callback is also called when the data waiting in the transmit buffer are successfully pushed to the PC Host and the transmit buffer free space increases. The prototype of the callback function provided by the user application must be as follows. The *PipeHandler* name is only a placeholder and must be defined by the application.

void PipeHandler(FMSTR\_HPIPE pipeHandle);

## FMSTR\_PipeClose

## **Prototype**

void FMSTR\_PipeClose(FMSTR\_HPIPE pipeHandle);

• Declaration: freemaster.h

• Implementation: freemaster\_pipes.c

## **Arguments**

• pipeHandle [in] - pipe handle returned from the FMSTR\_PipeOpen function call

**Description** This function de-initializes the pipe object. No data can be received or sent on the pipe after this call.

## FMSTR\_PipeWrite

## **Prototype**

FMSTR\_PIPE\_SIZE FMSTR\_PipeWrite(FMSTR\_HPIPE pipeHandle, FMSTR\_ADDR pipeData, FMSTR\_PIPE\_SIZE pipeDataLen, FMSTR\_PIPE\_SIZE writeGranularity);

• Declaration: freemaster.h

• Implementation: freemaster\_pipes.c

## **Arguments**

- pipeHandle [in] pipe handle returned from the FMSTR\_PipeOpen function call
- pipeData [in] address of the data to be written
- pipeDataLen [in] length of the data to be written
- writeGranularity [in] size of the minimum unit of data which is to be written

**Description** This function puts the user-specified data into the pipe's transmit memory buffer and schedules it for transmission. This function returns the number of bytes that were successfully written into the buffer. This number may be smaller than the number of the requested bytes if there is not enough free space in the transmit buffer.

The *writeGranularity* argument can be used to split the data into smaller chunks, each of the size given by the *writeGranularity* value. The FMSTR\_PipeWrite function writes as many data chunks as possible into the transmit buffer and does not attempt to write an incomplete chunk. This feature can prove to be useful to avoid the intermediate caching when writing an array of integer values or other multi-byte data items. When making the nGranularity value equal to the nLength value, all data are considered as one chunk which is either written successfully as a whole or not at all. The nGranularity value of 0 or 1 disables the data-chunk approach.

#### FMSTR\_PipeRead

#### **Prototype**

 $FMSTR\_PIPE\_SIZE\ FMSTR\_PipeRead (FMSTR\_HPIPE\ pipeHandle,\ FMSTR\_ADDR\ pipeData, \\FMSTR\_PIPE\_SIZE\ pipeDataLen,\ FMSTR\_PIPE\_SIZE\ readGranularity);$ 

- Declaration: freemaster.h
- Implementation: freemaster\_pipes.c

## **Arguments**

- pipeHandle [in] pipe handle returned from the FMSTR\_PipeOpen function call
- pipeData [in] address of the data buffer to be filled with the received data
- pipeDataLen [in] length of the data to be read
- readGranularity [in] size of the minimum unit of data which is to be read

**Description** This function copies the data received from the pipe from its receive buffer to the user buffer for further processing. The function returns the number of bytes that were successfully copied to the buffer. This number may be smaller than the number of the requested bytes if there is not enough data bytes available in the receive buffer.

The readGranularity argument can be used to copy the data in larger chunks in the same way as described in the FMSTR\_PipeWrite function.

**API data types** This section describes the data types used in the FreeMASTER driver. The information provided here can be useful when modifying or porting the FreeMASTER Communication Driver to new NXP platforms.

**Note:** The licensing conditions prohibit use of FreeMASTER and the FreeMASTER Communication Driver with non-NXP MPU or MCU products.

**Public common types** The table below describes the public data types used in the FreeMASTER driver API calls. The data types are declared in the *freemaster.h* header file.

8-bit value.

Type name	Description
	·
FM- STR_ADDR	Data type used to hold the memory address. On most platforms, this is normally a C-pointer, but it may also be a pure integer type.
For exam-	
ple, this type is	
defined as	
long inte-	
ger on the	
56F8xxx	
platform where	
the 24-bit	
addresses	
must be	
supported,	
but the C-pointer	
may be	
only 16	
bits wide	
in some	
compiler configura-	
tions.	
FM-	Data type used to hold the memory block size.
STR_SIZE It is re-	
quired	
that this	
type is un-	
signed and at least 16	
bits wide	
integer.	
FM-	Data type used as a general boolean type.
STR_BOOL This type	
is used	
only in	
zero/non-	
zero con- ditions in	
the driver	
code.	
FM-	Data type used to hold the Application Command code.
STR_APPCM. Generally,	
this is an	
unsigned	
8-bit value. <i>FM-</i>	Data time used to create the Application Command data buffer
STR_APPCM.	Data type used to create the Application Command data buffer.
Generally,	
this is an	
unsigned	
8-bit value. <i>FM</i> -	Data type used to hold the Application Command result code.
STR APPCM.	
<sup>2</sup> Generally,	Chapter 3. Middleware
this is an	
unsigned 8-bit value	

**Public TSA types** The table describes the TSA-specific public data types. These types are declared in the *freemaster\_tsa.h* header file, which is included in the user application indirectly by the *freemaster.h* file.

```
Data type used to hold a descriptor index in the TSA table or a table index in the
FM-
STR_TSA_TIl list of TSA tables.
By default,
this
         is
defined
       FM-
as
STR SIZE.
             Data type used to hold a memory block size, as used in the TSA descriptors.
FM-
STR\_TSA\_TSL
By default,
this
         is
defined
as
       FM-
STR_SIZE.
```

**Public Pipes types** The table describes the data types used by the FreeMASTER Pipes API:

FM- STR_HPIPE	Pipe handle that identifies the open-pipe object.
Generally, this is a pointer to a void type.	
FM- STR_PIPE_P(	Integer type required to hold at least 7 bits of data.
Generally, this is an unsigned 8-bit or 16-bit type.	
FM- STR_PIPE_SI	Integer type required to hold at least 16 bits of data.
This is used to store the data buffer sizes.	
FM- STR_PPIPEF	Pointer to the pipe handler function.
See FM- STR_PipeOpe for more details.	

**Internal types** The table describes the data types used internally by the FreeMASTER driver. The data types are declared in the platform-specific header file and they are not available in the application code.

EMCED III	ml 11
FMSTR_U8 On the vast	The smallest memory entity.
majority of	
platforms,	
this is an	
unsigned	
8-bit inte-	
ger.	
On the	
56F8xx	
DSP plat-	
form, this	
is defined	
as an un-	
signed	
16-bit inte-	
ger.	Unaigned 16 hit integer
FM-	Unsigned 16-bit integer.
STR_U16 FM-	Unsigned 32-bit integer.
STR_U32	onsigned 32 bit integer.
FMSTR_S8	Signed 8-bit integer.
FM-	Signed 16-bit integer.
STR_S16	
FM-	Signed 32-bit integer.
STR_S32	Alasta standard IEEE Continuo sint tama
FM-	4-byte standard IEEE floating-point type.
STR_FLOAT FM-	Data type forming a union with a structure of flag bit-fields.
STR_FLAGS	Butta type forming a timori with a structure of mag bit netas.
FM-	Data type holding a general size value, at least 8 bits wide.
STR_SIZE8	
FM-	General for-loop index. Must be signed, at least 16 bits wide.
STR_INDEX	
FM-	A single character in the communication buffer.
STR_BCHR	
Typically, this is	
an 8-bit	
unsigned	
integer,	
except for	
the DSP	
platforms	
where it	
is a 16-bit	
integer.	
FM-	A pointer to the communication buffer (an array of FMSTR_BCHR).
STR_BPTR	

## **Document references**

## Links

• This document online: https://mcuxpresso.nxp.com/mcuxsdk/latest/html/middleware/freemaster/doc/index.html

- FreeMASTER tool home: www.nxp.com/freemaster
- FreeMASTER community area: community.nxp.com/community/freemaster
- FreeMASTER GitHub code repo: https://github.com/nxp-mcuxpresso/mcux-freemaster
- MCUXpresso SDK home: www.nxp.com/mcuxpresso
- MCUXpresso SDK builder: mcuxpresso.nxp.com/en

#### **Documents**

- FreeMASTER Usage Serial Driver Implementation (document AN4752)
- Integrating FreeMASTER Time Debugging Tool With CodeWarrior For Microcontrollers v10.X Project (document AN4771)
- Flash Driver Library For MC56F847xx And MC56F827xx DSC Family (document AN4860)

**Revision history** This Table summarizes the changes done to this document since the initial release.

Revi- sion	Date	Description
1.0	03/2006	Limited initial release
2.0	09/2007	Updated for FreeMASTER version. New Freescale document template used.
2.1	12/2007	Added description of the new Fast Recorder feature and its API.
2.2	04/2010	Added support for MPC56xx platform, Added new API for use CAN interface.
2.3	04/2011	Added support for Kxx Kinetis platform and MQX operating system.
2.4	06/2011	Serial driver update, adds support for USB CDC interface.
2.5	08/2011	Added Packet Driven BDM interface.
2.7	12/2013	Added FLEXCAN32 interface, byte access and isr callback configuration option.
2.8	06/2014	Removed obsolete license text, see the software package content for up-to-date license.
2.9	03/2015	Update for driver version 1.8.2 and 1.9: FreeMASTER Pipes, TSA Active Content, LIN Transport Layer support, DEBUG-TX communication troubleshooting, Kinetis SDK support.
3.0	08/2016	Update for driver version 2.0: Added support for MPC56xx, MPC57xx, KEAxx and S32Kxx platforms. New NXP document template as well as new license agreement used. added MCAN interface. Folders structure at the installation destination was rearranged.
4.0	04/2019	Update for driver released as part of FreeMASTER v3.0 and MCUXpresso SDK 2.6. Updated to match new V4 serial communication protocol and new configuration options. This version of the document removes substantial portion of outdated information related to S08, S12, ColdFire, Power and other legacy platforms.
4.1	04/2020	Minor update for FreeMASTER driver included in MCUXpresso SDK 2.8.
4.2	09/2020	Added example applications description and information about the MCUXpresso Config Tools. Fixed the pipe-related API description.
4.3	10/2024	Added description of Network and Segger J-Link RTT interface configuration. Accompanying the MCUXpresso SDK version 24.12.00.
4.4	04/2025	Added Zephyr-specific information. Accompanying the MCUXpresso SDK version 25.06.00.

# **Chapter 4**

# **RTOS**

## 4.1 FreeRTOS

## 4.1.1 FreeRTOS kernel

Open source RTOS kernel for small devices.

FreeRTOS kernel for MCUXpresso SDK Readme

FreeRTOS kernel for MCUXpresso SDK ChangeLog

FreeRTOS kernel Readme

## 4.1.2 FreeRTOS drivers

This is set of NXP provided FreeRTOS reentrant bus drivers.

# 4.1.3 backoffalgorithm

Algorithm for calculating exponential backoff with jitter for network retry attempts.

## Readme

## 4.1.4 corehttp

C language HTTP client library designed for embedded platforms.

## 4.1.5 corejson

JSON parser.

## Readme

# 4.1.6 coremqtt

MQTT publish/subscribe messaging library.

# 4.1.7 coremqtt-agent

The coreMQTT Agent library is a high level API that adds thread safety to the coreMQTT library.

## Readme

# 4.1.8 corepkcs11

PKCS #11 key management library.

## Readme

# 4.1.9 freertos-plus-tcp

Open source RTOS FreeRTOS Plus TCP.

## Readme

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